Power Quality Deterioration due Complex Behavior of a Power Inverter With a Three-Phase-Resistive Load

N. Toro, Y. A. Garcés and F. E. Hoyos.

Abstract—**This paper shows the behavior of a three-phase power converter with resistive load using a quasi-sliding control technique for output voltage regulation and a chaos control technique. Controller is designed using Zero Average Dynamic (ZAD) and Fixed Point Inducting Control (FPIC) techniques. Designs have been tested in a Rapid Control Prototyping (RCP) system based on Digital Signal Processing (DSP) for dSPACE platform. Bifurcation diagrams show the robustness of the system. Chaos detection is a signal processing method in the time domain, and has power quality phenomena detection applications. Results show that the phase voltage in the load has sinusoidal performance when it is controlled with these techniques. When delay effects are considered, experimental and numerical results match in both of stable and transition to chaos zones.**

Index terms— **Power measurement, Power quality, Power electronics, Complexity theory, Chaos, Power Inverter.**

I. Introduction

STUDY of variable structure systems uses bifurcation theory in order to determine the conditions in parameters values which generate stability changes, periodicity and chaotic dynamics in the system, allow us to define safe and stable operation zones. Knowledge of these operation ranges lets us avoid the presence of non-desired phenomena such as auto-sustained oscillations, chaos, and evolution to other operation regimes, among others.

Control action required for three-phase loads is implemented usually by power electronics circuit based on switches. For this reason, controlled commuted system with three-phase-load (Resistive) becomes a variable structure system defined by non-smooth differential equations in which a complete theoretical framework does not exist yet that allows its study [1]-[2] since its theoretical and numerical analysis represents a extremely difficult problem [3]. In this sense, non-smooth transitions occur when a cycle interact with a boundary of discontinuity in the phase space in a non-generic way, causing periodic additions or sudden chaos transitions [4]. One of the most relevant aspects in the bifurcation analysis of non-smooth systems is the absence of the double periodic sequences that are observed in smooth systems [3]. Due of characteristic behavior of non-smooth systems, in many cases, it is no possible to apply analysis techniques for smooth systems without modifications or adequate adjustments [1].

Converters use power electronics for efficient transformation and rational use of electricity from the generation sources to its industrial and commercial use. It has been estimated that 90% of electrical energy is processed through power converters before the final use [5]. Power converters must provide certain level of output voltage, either in tasks regulation or tracking, and they must be able to reject changes in load and primary supply voltage levels. A complete and detailed analysis of the operation and configuration of different power converters can be found in [6]- [7]. One of the most desirable qualities in these devices is efficiency in the performance by using switching devices generating the desired output with low power consumption.

In general, the deterioration of power quality is due to non-stationary disturbances (voltage sags, voltage swells, impulses, among others) and also due to stationary disturbances (harmonic distortion, unbalance and flicker) [8]-[11]. In addition, the chaotic dynamics in the system under study generate non-periodic solution currents that are reflected on the source side, affecting another ones sensitive loads connected to the point of common coupling.

Controller designed in the this work combines Zero Average Dynamics (ZAD) and Fixed Point Inducting Controller (FPIC) strategies, which have been reported in [12] -[18]. Design corresponds to a three-phase low power inverter (1500 W) with three phase resistive load using a dSPACE platform for the control. Numerical and experimental bifurcations are obtained for the ZAD-FPIC-controller, by changing the parameter values. Obtained numerical and

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N. Toro is with the Department of Electrical, Electronic and Computer Engineering, Universidad Nacional de Colombia, Manizales–Colombia and the Department of Electronics and Automation, Universidad Autónoma de Manizales, Manizales - Colombia (corresponding author: Tel: +57 6 8879400 int. 55817,e-mail: ntoroga@unal.edu.co).
Y. A. Garcés-Gómez is with the Universidad Nacional de Colombia, Manizales – Colombia (e-mail: yagarsesg@unal.edu.co).
F. E. Hoyos is with the Department of Engineering, Instituto Tecnológico de Antioquia, Medellin - Colombia(e-mail: fehoyosv@gmail.com).

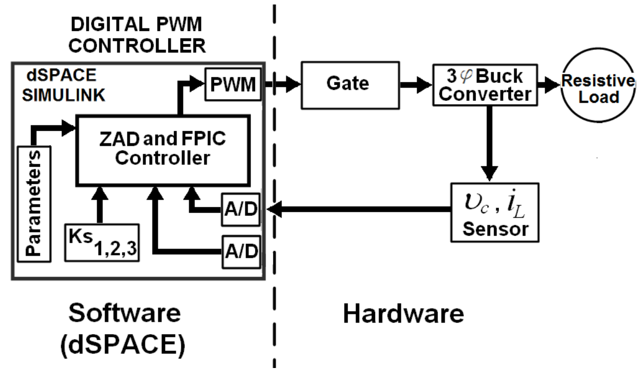


Fig. 1. Block Diagram of the proposed system.

experimental bifurcation diagrams match. Development and application of the FPIC control technique are presented in [14]-[15], [17]-[18]. This technique allows the stabilization of unstable orbits in a simple way.

This paper is organized as follows. Section II describes the proposed system. Section III describes the mathematical model of the system. Section IV describes the control techniques. Section V presents the obtained results, and finally, section VI presents the conclusion.

II. Proposed System

Figure 1 shows the block diagram of the system under study. This system is divided into two major subgroups, hardware and software. Hardware includes electrical circuits and electronic devices, and software includes signals acquisition and implementation of control techniques. The software is implemented in a dSPACE platform.

Hardware is composed of a Three–phase power converter with resistive load wich is rated to 1500W, 600 V DC and 20 A DC. For the measure of variables, υ_c (capacitor voltage), a series resistance was used and for the measurement of i_L (inductor currents) HX10P/SP2 current sensors were used. Converter switches were driven by PWM outputs of the controller card; these signals are coupled via fast optocouplers (6N137).

Software is developed using the control and development card dSPACE DS1104, where ZAD and FPIC control techniques are implemented. The sampling rate for all variables is set to 6kHz. The state variables υ_c and i_L are stored at 12 bits; the duty cycle (d) is handled at 10 bits. Parameters of buck converter (C , L , r_s , r_L) and ZAD-FPIC–controller (K_S , N , F_S , R) are entered to the control block by the user, as constant parameters. K_S is the bifurcation parameter. For each sample the controller calculates in real time the duty cycle and the equivalent PWM signal to control the gate.

III. Mathematical Model

Figure 2 shows a basic diagram of the system. Buck power converter is used to feed the resistive load. Equation (1) is obtained for the system model.

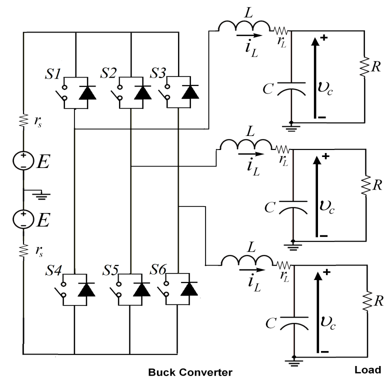


Fig. 2. Electrical circuit for the buck-motor system.

$$\begin{bmatrix} \dot{v}_{c_a} \\ \dot{i}_{L_a} \\ \dot{v}_{c_b} \\ \dot{i}_{L_b} \\ \dot{v}_{c_c} \\ \dot{i}_{L_c} \end{bmatrix} = \begin{bmatrix} \frac{-1}{R_a C_a} & \frac{1}{C_a} & 0 & 0 & 0 & 0 \\ \frac{-1}{L_a} & \frac{-(r_s + r_{L_a})}{L_a} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{R_b C_b} & \frac{1}{C_b} & 0 & 0 \\ 0 & 0 & \frac{-1}{L_b} & \frac{-(r_s + r_{L_b})}{L_b} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{R_c C_c} & \frac{1}{C_c} \\ 0 & 0 & 0 & 0 & \frac{-1}{L_c} & \frac{-(r_s + r_{L_c})}{L_c} \end{bmatrix} \begin{bmatrix} v_{c_a} \\ i_{L_a} \\ v_{c_b} \\ i_{L_b} \\ v_{c_c} \\ i_{L_c} \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ \frac{E}{L_a} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & \frac{E}{L_b} & 0 \\ 0 & 0 & 0 \\ 0 & 0 & \frac{E}{L_c} \end{bmatrix} \begin{bmatrix} S_1 - S_4 \\ S_2 - S_5 \\ S_3 - S_6 \end{bmatrix} \quad (1)$$

with

$$S_4 = 1 - S_1$$
$$S_5 = 1 - S_2$$
$$S_6 = 1 - S_3$$

and

$$S_i \in \{0,1\}$$
$$for\ i = 1 \ldots 6$$

This equation can be expressed in a compact form as:

$$\dot{x} = Ax + BU \quad (2)$$

where the state variables are:

$$v_{c_a} = x_1,\ i_{L_a} = x_2,\ v_{c_b} = x_3,\ i_{L_b} = x_4,\ v_{c_c} = x_5,\ and\ i_{L_c} = x_6$$

A is a block diagonal matrix, so that the system consists of three uncoupled subsystems that may be treated independently. Figure 3 shows the equivalent circuit per phase.

A. Derivation of the discrete time iterative map of the converter

The inherent piecewise switched operation converters implies a multi-topological mode in which one particular circuit topology describes the system for a particular interval of time. The first step in the analysis of multi-topological circuit is to write down the state equations, which describes the individual switched circuits. For converters operating in continuous conduction mode, two switched circuits can be

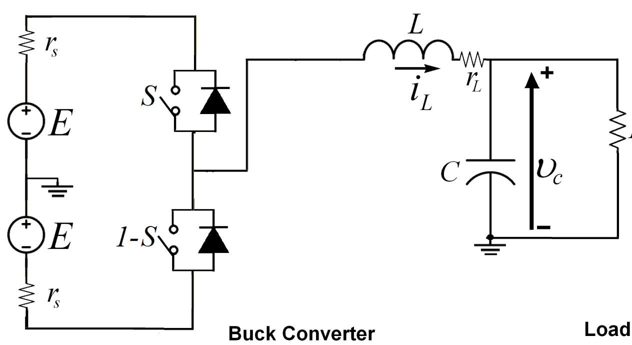


Fig. 3. Electrical circuit for the buck converter (equivalent per phase)

identified. When the switch is ON, it is described by equation (3); when the switch is OFF, it is described by equation (4).

$$\begin{bmatrix} \dot{\upsilon}_c \\ i_L \end{bmatrix} = \begin{bmatrix} \frac{-1}{RC} & \frac{1}{C} \\ \frac{-1}{L} & \frac{-(r_s+r_L)}{L} \end{bmatrix} \begin{bmatrix} v_c \\ i_L \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{E}{L} \end{bmatrix} \quad (3)$$

$$\begin{bmatrix} \dot{\upsilon}_c \\ i_L \end{bmatrix} = \begin{bmatrix} \frac{-1}{RC} & \frac{1}{C} \\ \frac{-1}{L} & \frac{-(r_s+r_L)}{L} \end{bmatrix} \begin{bmatrix} v_c \\ i_L \end{bmatrix} + \begin{bmatrix} 0 \\ -\frac{E}{L} \end{bmatrix} \quad (4)$$

State variables are the capacitor voltage (υ_c) and the inductor current (i_L). These equations can be expressed in a compact from as $\dot{x} = Ax + Bu$ with $x_1 = v_C$ and $x_2 = i_L$. E denotes the converter power supply and depending on the control pulse voltage E or $-E$ is injected to the system through a PWM signal.

By considering continuous conduction mode (CCM) and according to centered PWM (Figure 4), the control signal is defined as follows (5):

$$u = \begin{cases} 1 & \text{if} \quad kT \le t \le kT + dT/2 \\ -1 & \text{if} \quad kT + dT/2 < t < kT + T - dT/2 \\ 1 & \text{if} \quad kT + T - dT/2 < t < kT + T \end{cases} \quad (5)$$

Solution of the system (3) for $kT < t < (kT + dT/2)$ is given by:

$$x(t) = e^{A(t-kT)}x(kT) - A^{-1}[I - e^{A(t-kT)}]B$$

Solution of the system (4) for $(kT + dT/2) < t < (kT + T - dT/2)$ is given by:

$$x(t) = e^{A(t-(kT+dT/2))}x(kT + dT/2) + A^{-1}[I - e^{A(t-(kT+dT/2))}]B$$

where

$$x(kT + dT/2) = e^{A(dT/2)}x(kT) - A^{-1}[I - e^{A(dT/2)}]B$$

The solution of the system (3) for $(kT + T - dT/2) < t < (kT + T)$ is given by:

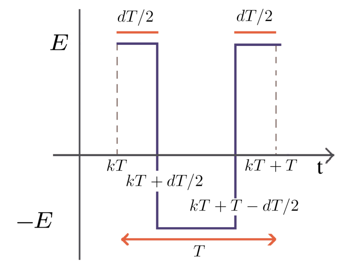


Fig. 4. Centered PWM

$$x(t) = e^{A(t-(kT+T-dT/2))}x(kT + T - dT/2) - A^{-1}[I - e^{A(t-(kT+T-dT/2))}]B$$

where

$$x(kT + T - dT/2) = e^{A(T-dT)}x(kT + dT/2) + A^{-1}[I - e^{A(T-dT)}]B$$

General solution of the system for $kT < t < (kT + T)$ is given by

$$x((k+1)T) = e^{AT}x(kT) + [2e^{A(dT/2)} - 2e^{A(T-dT/2)} + e^{AT} - I]A^{-1}B \quad (6)$$

where k represents the k^{th} iteration, T is the sampling period and d is the duty cycle.

Equation (6) is the *discrete-time state equation* for the buck converter. In much of the literature, the terms *iterative map, iterative function* and *Poincaré map* have been used synonymically with *discrete-time state equation*.

IV. Control Strategies

The control strategies presented in this section are developed for the per phase equivalent circuit. So for the three phase system the control must be applied for each phase independently, taking into account that the reference voltage will be phase shifted according to the corresponding circuit phase.

A. ZAD control strategy

As reported in [19][20][21], one of the possibilities for computing the duty cycle is to define a surface and to force it to be zero in each iteration. The surface per phase is defined as a piecewise-linear function given by

$$s_{pwl}(t) = \begin{cases} s_1 + (t - kT)\dot{s}_+ & \text{if} \quad kT \le t \le t_1 \\ s_2 + (t - kT + \frac{d_k}{2})\dot{s}_- & \text{if} \quad t_1 < t < t_2 \\ s_3 + (t - kT + T + \frac{d_k}{2})\dot{s}_+ & \text{if} \quad t_2 \le (k+1)T \end{cases} \quad (7)$$

where the variables are described in (8)

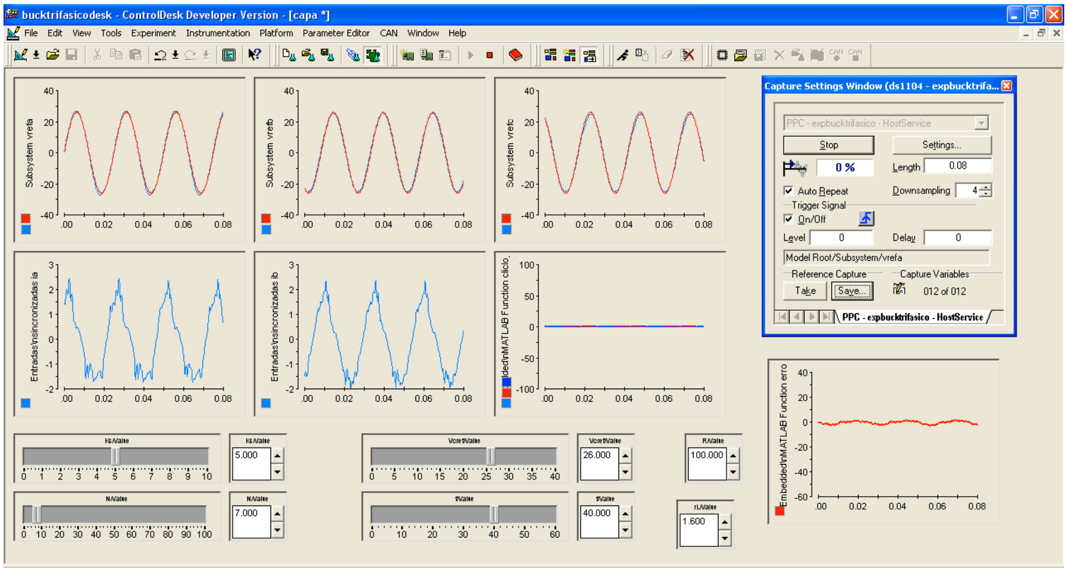


Fig. 5. Periodic Solution for the Three–phase converter with resistive load

$$\begin{aligned}
\dot{s}_+ &= ((\dot{x}_1 - \dot{x}_{ref}) + k_s(\ddot{x}_1 - \ddot{x}_{ref}))\big|_{x=x(kT),u=1} \\
\dot{s}_- &= ((\dot{x}_1 - \dot{x}_{ref}) + k_s(\ddot{x}_1 - \ddot{x}_{ref}))\big|_{x=x(kT),u=-1} \\
s_1 &= ((x_1 - x_{ref}) + k_s(\dot{x}_1 - \dot{x}_{ref}))\big|_{x=x(kT),u=1} \\
s_2 &= \frac{d_k}{2}\dot{s}_1 + s_1 \\
s_3 &= s_1 + (T - d_k)\dot{s}_2 \\
t_1 &= kT + \frac{d_k}{2} \\
t_2 &= kT + (T - \frac{d_k}{2}) \\
t_3 &= (k+1)T
\end{aligned} \tag{8}$$

with $k_s = Ks * \sqrt{LC}$ a positive constant.

The d_k satisfying zero average requirements is:

$$D_k = \frac{2s_1(x(kT)) + T\dot{s}_-(x(kT))}{\dot{s}_-(x(kT)) - \dot{s}_+(x(kT))} \tag{9}$$

From (3), (4) and (8) we obtain

$$\begin{aligned}
s_1(kT) &= (1 + ak_s)x_1(kT) + bk_s x_2(kT) - x_{1ref} - k_s\dot{x}_{1ref} \\
\dot{s}_+(kT) &= (a + a^2k_s + bck_s)x_1(kT) + (b + abk_s + bdk_s)x_2(kT) + bk_s\frac{E}{L} - \dot{x}_{1ref} - k_s\ddot{x}_{1ref} \\
\dot{s}_-(kT) &= (a + a^2k_s + bck_s)x_1(kT) + (b + abk_s + bdk_s)x_2(kT) - bk_s\frac{E}{L} - \dot{x}_{1ref} - k_s\ddot{x}_{1ref}
\end{aligned} \tag{10}$$

with $a = -\frac{1}{RC}$, $b = \frac{1}{C}$, $c = -\frac{1}{L}$, $d = -\frac{(r_s + r_L)}{L}$

The duty cycle is given by (11).

$$d_k = \begin{cases} 1 & \text{if} \quad D_k > T \\ D_k / T & \text{if} \quad 0 \le D_k \le T \\ 0 & \text{if} \quad D_k < 0 \end{cases} \tag{11}$$

We have experimentally measured and noticed that there is a period delay in the control action. In this case, the control action is taken from the data acquired in the past sampling time, and then we compute the duty cycle as:

$$d_k = \frac{2s_1(x(k-1)T) + T\dot{s}_-(x(k-1)T)}{\dot{s}_-(x(k-1)T) - \dot{s}_+(x(k-1)T)} \tag{12}$$

To apply this technique we need to measure the states at the beginning of each sampling time. For doing this, we carry out a synchronization between the measured signals and the start of the PWM. This synchronization is performed using a trigger signal obtained from the PWM, which gives the command to ADC converter for reading v_C and i_L. On the other hand, we need to know the values of the parameters L, C, r_S, r_L. In this case, we suppose that these parameters will be constant and measurable. The load R may be unknown and in this case must be estimated.

Taking into account the strategies FPIC and ZAD, the new duty cycle is calculated as follow:

$$d_{k-FPIC} = \frac{d_k(k) + N \cdot d^*}{N+1} \tag{13}$$

Where $d_K(k)$ is calculated as (12) and d^* is the calculated duty cycle in steady state $(x_1(kT) = x_{1ref})$. From (9)

$$d^* = D_k\big|_{x_1(kT)=x_{1ref}} = \frac{T}{2} + \frac{T[(1 + \frac{r_s + r_L}{R})x_{1ref} + (\frac{L}{R} + (r_s + r_L)C)\dot{x}_{1ref} + LC\ddot{x}_{1ref}]}{2E} \tag{13}$$

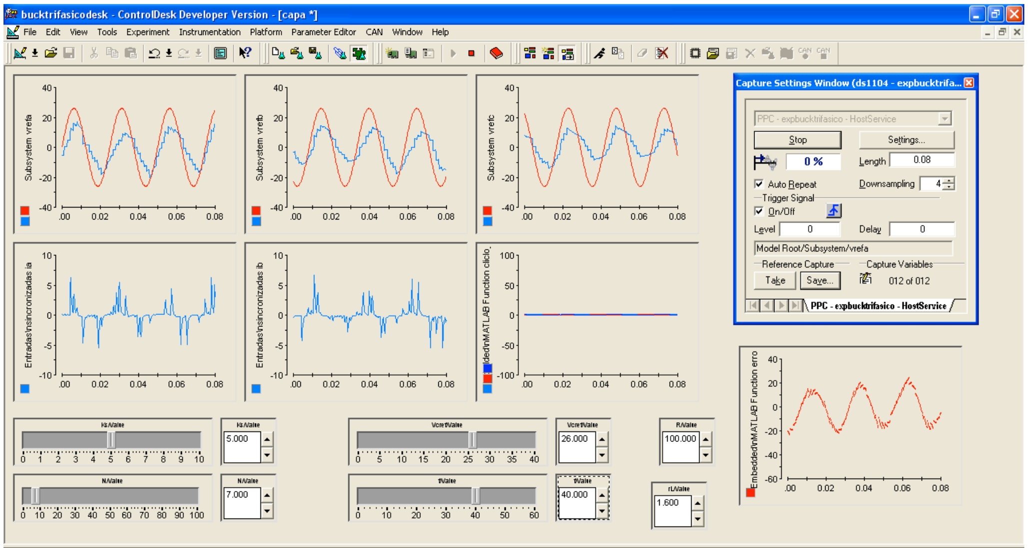


Fig. 6. Chaotic Solution for the Three–phase converter with resistive load

V. Numerical and Experimental Results

In this section numerical and experimental results are shown using K_S and N as bifurcation parameters, in addition the system behavior under frequency and voltage amplitude variations are illustrated graphically. Parameter values used in simulations and experiments are listed in Table I, initially the reference voltage has a peak of 32V and 40Hz of frequency. For the simulation in SIMULINK model the fixed step size (fundamental sample time) in configuration parameter was setting in $1/(4Fs)$.

TABLE I
Units for Magnetic Properties

Parameter	Value
r_S : Internal resistance of the source	4Ω
E : Input voltage	40V
L : Inductance	1.6mH
r_L : Internal resistance of the inductor	0.9Ω
C : Capacitance	368uF
N : FPIC control parameter	7
Fc : Switching frequency	4kHz
Fs : Sampling frequency	4kHz
$1T\_p$: 1 Delay time	0.25ms
K_S : Control parameters	5

Figures 5 and 6 shows the experimental behavior for the Three–phase power converter, using the same parameters and controller, but with different initial conditions. References Voltages for phases a, b, c (red signals); phase voltages (v_a, v_b, v_c) and phase currents (i_a, i_b) (blue signals) are shown in these Figures.

In Figure 5 the system exhibits a periodic solution and in Figure 6 a chaotic solution. This fact shows the coexistence of attractors or solutions in the system. When the solution is periodic, the controlled voltage follows the voltage reference by the control action unlike the chaotic solution, where the output voltage is lower than the reference and it has an irregular fashion, in this regime the phase currents have a higher peak. Some times the system toggles between two

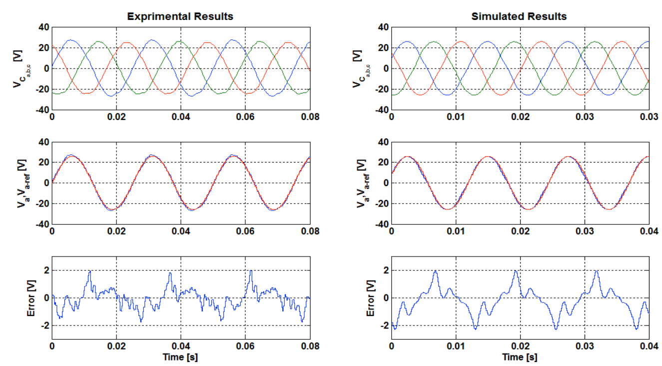


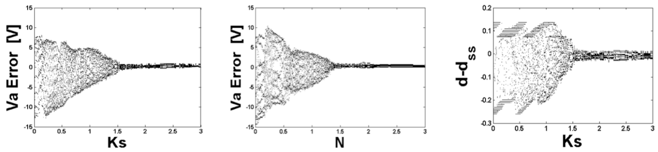
Fig. 7. Experimental and simulation results for Three–phase converter with resistive load

solutions while it is running, this happens when the solution is near of the border of two regions of attraction.

Results obtained in simulation and experiments for periodic solution are shown in Figure 7. The simulation was executed taking into account a 3T (0,75ms) delay in the duty cycle application. Under this condition simulation and experimental results match. Controlled voltage v_C follows reference voltage for all phases with a maximum error of 2V.

Figure 8 shows the bifurcation diagrams for the output error and duty cycle of controlled system with K_S and N like bifurcation parameters, obtained via model simulation using Simulink of Matlab. For $K_S = 1{,}5$ with $N = 2$ and $N = 1{,}5$ with $K_S = 3$ the system presents a qualitatively behavior change. Before $K_S = 1{,}5$ and $N = 1{,}5$ the system is in chaotic regime and after is in stable regime. For constructing these diagrams, the simulation was running for 3 periods of reference voltage and the last 15 samples of output error are taken with initial conditions equal to zero; also a delay in duty cycle application of 3T.

In next the results of experiments are shown for buck power converter behavior when the voltage reference and voltage level vary.



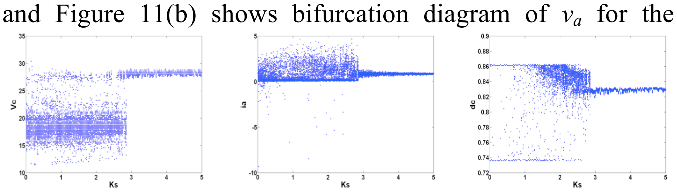
(a) Bifurcation Diagram with $N = 2$ (b) Bifurcation Diagram with $Ks = 3$ (c) Bifurcation Diagram with $N = 2$

Fig. 8. Error in voltage, with ks and N like bifurcation parameters, and error in duty cycle for phase a resulting from the model simulation using Simulink of Matlab of Three– phase converter with resistive load..

Figure 9 shows the bifurcation diagrams for the output error and duty cycle of the controlled system with KS and N as bifurcation parameters, obtained experimentally. For $K_S = 3$ the system presents a qualitatively behavior change. Before $K_S = 3$ the system is in chaotic regime and after is in stable regime. For constructing these diagrams, the experiment was run for 2 seconds for each value of Ks and samples were acquired every 50 milliseconds.

Figure 10 shows the bifurcation diagrams for the i_a current, v_a voltage and duty cycle of controlled system with f (frequency of voltage reference) like bifurcation parameter, obtained experimentally. For $f \approx 27Hz$ the system presents a qualitatively behavior change. After $f = 27Hz$ the system is chaotic regime and before is stable regime. For constructing these diagrams, the experiment was run for 2 seconds for each value of *f* and samples were acquired every 50 milliseconds. Phenomenon shown in Figure 4.10 is caused by saturation of the inductor core in the *LC* filter; due the core saturation and magnetic hysteresis not were simulated these phenomena are not present in simulations.

Figure 11(a) shows the bifurcation diagram of duty cycle and Figure 11(b) shows bifurcation diagram of v_a for the



(a) v_c Bifurcation Diagram (b) i_a Bifurcation Diagram (c) Duty cycle Bifurcation Diagram

Fig. 9. v_c voltage, i_a current and duty cycle experimental bifurcation diagrams with K_S like bifurcation parameter of three phasic converter with resistive load.

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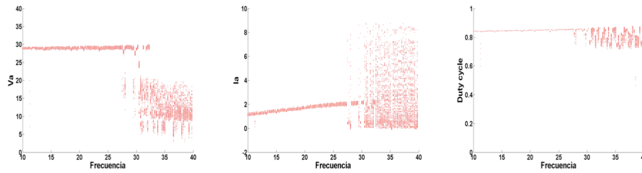
Poincare map (6), both of which are numerical. Bifurcation diagrams were constructed taking the last 30 samples, each one every period of reference voltage for phase *a* from the model (6) simulation using Matlab, while the system was running during 35 periods. The simulation was executed taking into account a single period (1T) of delay in the duty cycle application. In these Figures various regimes of operation can be appreciated: periodic windows, Chaos and periodic solutions.

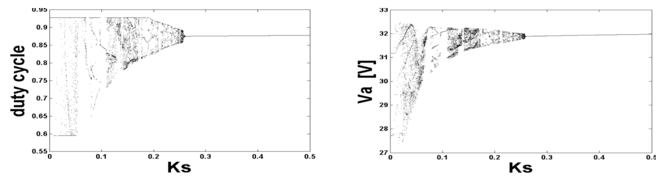
The Figure 12 shows the bifurcation diagram when 3T of delay is considered. Bifurcation diagrams are quite different for different delay.

Before analysis shows the effects of the delay time in the signal control applied to the power converter. Many complex



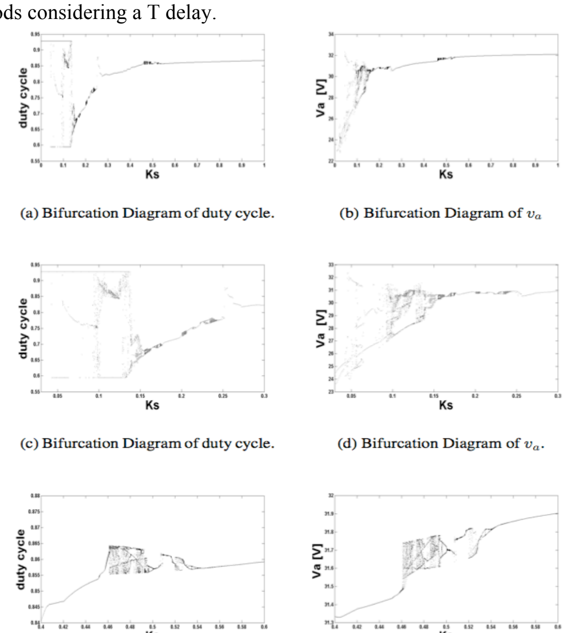
(a) v_a Bifurcation Diagram (b) i_a Bifurcation Diagram (c) Duty cycle Bifurcation Diagram

Fig. 10. *Vc* voltage, ia current and duty cycle experimental bifurcation diagrams with f like bifurcation parameter of three phasic converter with resistive load.



(a) Bifurcation Diagram of duty cycle for the Poincare map 4.6 (b) Bifurcation Diagram of v_a error for the Poincare map 4.6

Fig. 11. Bifurcation Diagram with *Ks* like bifurcation parameters, taking one sample each period of the reference voltage for phase a during 30 periods considering a T delay.



(a) Bifurcation Diagram of duty cycle. (b) Bifurcation Diagram of v_a

(c) Bifurcation Diagram of duty cycle. (d) Bifurcation Diagram of v_a.

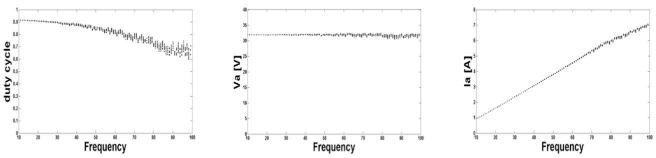
(e) Bifurcation Diagram of duty cycle. (f) Bifurcation Diagram of v_a

Fig. 12. bifurcation Diagram with *Ks* like bifurcation parameters, Taking a sample each 30 periods of the reference voltage for phase a considering a 3T delay, for the Poincare map 4.6.

phenomena arise like shown in Figures 12(e) and 12(f) some of these are no smooth bifurcations, double period bifurcations, chaos and 1-periodic orbits.

In order to analyze the effect of the variation of frequency and voltage level in the reference voltage, a simulation was carried out.

Results obtained varying the frequency of reference voltage are shown in Figure 13. The Figures 13(a), 13(b), 13(c) show the behavior of duty cycle, peak voltage and peak current in C and L respectively when the frequency voltage reference is varied in the Poincare map simulation. The amplitude of the output voltage does not drops significantlly with the variation of frequency, but the current peak has a linear growth with



(a) duty cycle. (b) v_a peak. (c) i_a peak.

Fig. 13. Results for Poincare map 4.6 simulation, Taking a sample on each one of last 10 periods of the reference voltage for phase a and ia considering a3T delay,varying frequency in the reference voltage.

frequency, shown a predominant capacitive effect. In this case the delay has not a significant impact.

VI. Conclusion

Control strategy ZAD-FPIC was designed and applied to three phase buck converter with resistive load. For this system, simulations and experiments were performed. The stability of the closed loop system was analyzed using bifurcation diagrams; stability and transitions to chaos were observed. It was demonstrated in an experimental way, that the delay effects have high importance in ZAD strategy. Simulations and experiments match when delay effects were included and improving the quality of the waves with ZAD control. Thus, in the chaos zone, it was observed power quality deterioration by non periodical current and voltage waveforms, but, when the control is performed the non-periodicity is eliminated.

References

[1]. M. diBernardo and C. Budd and A. R. Champaynes and P. Kowalczy and A. B. Nordmark and G. Olivar and P. T Piiroinen, "Bifurcatios in Nonsmooth Dynamical Systems",*AMS Subject Classifications: 34A36, 34D08, 37D45, 37G15, 37N05, 37N20*, May. 2006.

[2]. M. diBernardo and C. Budd and A. R. Champaynes and P. Kowalczyk, "Piecewise-smooth Dynamical Systems: Theory and Applications", *Springer*, New York, 2007.

[3]. Z. T. Zhusubaliyev and E. Mosekilde, "Bifurcations and Chaos in Piecewise-Smooth Dynamical Systems," *World Scientific, series on Nonlinear sciencE, A*, vol. 44, London. 2003.

[4]. P. Kowalczyk and M. DiBernardo and A. R. Champneys and S. J. Hogan and M. Hommer and P. T. Phroinen and Y. A. Kuznetsov and A. Nordmark, "Two-Parameter discontinuity-Induced bifurcations of cycles: Classification And open Problems," *International Journal of Bifurcation and Chaos*., vol. 16, no. 3, Jan. 2006.

[5]. S. Banerjee and G.C. Verghese, "Nonlinear phenomena in power electronics," *IEEE Press. Piscataway.*, 2001.

[6]. N. Mohan and T. Undeland and W. Robbins, "Power Electronics: Converters. Aplications and Design", *J. Wiley.*, 1995.

[7]. N. Mohan, "First Course on Power Electronics and drives," *Mnpere, USA.*, 2003.

[8]. T. Lin and A. Domijan, "On power quality indices and real time measurement," *IEEE Trans. Power Del*., vol. 20, no. 4, pp. 2552–2562, Oct. 2005.

[9]. A. Ferrero, "Measuring Electric Power Quality: Problems and Perspectives", *Measurement*, vol. 41, no 2, pp.121-129, Feb. 2008, doi: 10.1016/j.measurement.2006.03.004.

[10]. P. Salmerón, R.S. Herrera, A. Pérez and J. Prieto, "New Distortion and Unbalance Indices Based on Power Quality Analyzer Measurements," *IEEE Trans. Power Del*., vol. 24, no. 2, Apr. 2009.

[11]. Y.J. Shin, E.J. Powers, M. Grady, and A. Arapostathis, "Power Quality Indices for Transient Disturbances," *IEEE Trans. Power Del*., vol. 21, no. 1, Jan. 2006.

[12]. E. Fossas and R. Griñó and D. Biel, "Quasi-Sliding Control based on Pulse Width Modulation. Zero Averaged Dynamics and the L2 Norm," *Advances in Variable Structure Systems. Analysis. Integration and Applications (6th International Workshop on Variable Structure Systems (VSS'2000).*, pp. 335-344, 2000.

[13]. F. Angulo and G. Olivar and J.A. Taborda, "Continuation of periodic orbits in a ZAD-strategy controlled buck converter," *Chaos. Solitons and Fractals.*, Vol. 38, pp. 348-363, 2008.

[14]. F. Angulo and E. Fossas and G. Olivar, "Transition from periodicity to chaos in a PWM controlled buck converter with ZAD strategy," *Int. Journal of Bifurcations and Chaos.*, Vol. 15, pp. 3245-3264, 2005.

[15]. F. Angulo., "Análisis de la dinámica de convertidores electrónicos de potencia usando PWM basado en promediado cero de la dinámica del error (ZAD)," *Universidad Politécnica de Cataluña, Cataluña*., 2004.

[16]. J. Taborda., "Análisis de bifurcaciones en sistemas de segundo orden usando pwm y promediado cero de la dinámica del error," *Universidad Nacional de Colombia - Sede Manizales*., Colombia, Mayo 2006.

[17]. F. Angulo and J.E. Burgos and G. Olivar., "Chaos stabilization with TDAS and FPIC in a buck converter controlled by lateral PWM and ZAD," *In Proceedings: Mediterranean Conference on Control and Automation.*, July 2007.

[18]. F. Angulo, and G. Olivar, and J. Taborda, and F. Hoyos., "Nonsmooth dynamics and FPIC chaos control in a DC-DC ZAD-strategy power converter," *EUROMECH Nonlinear Dynamics Conference*., Saint Petersburg, RUSSIA, July 2008.

[19]. F. Angulo, G. Olivar, and J. Taborda, "Continuation of periodic orbits in a zad-strategy con- trolled buck converter," *Chaos. Solitons and Fractals*, vol. 38, pp. 348–363, 2008.

[20]. F. Angulo, "Análisis de la dinámica de convertidores electrónicos de potencia usando pwm basado en promediado cero de la dinámica del error (zad)," Ph.D. dissertation, Universidad Politécnica de Cataluña, Cataluña, 2004.

[21]. J. Taborda, "Análisis de bifurcaciones en sistemas de segundo orden usando pwm y promedi- ado cero de la dinámica del error," Master's thesis, Universidad Nacional de Colombia - Sede Manizales, Colombia, Mayo 2006.

Authors

Yeison A. Garces-Gomez: was born in Manzanares-Caldas, Colombia, in 1983. He received the B.Sc. Engineering degree in 2009 from National University of Colombia, Manizales Branch, in electronic engineering. Between 2009 and 2011 had a "Colciencias" scholarship for postgraduate studies in engineering - industrial automation at the National University of Colombia. He is currently working for Ph.D degree in engineering in the National University of Colombia. His research interests include power definitions under nonsinusoidal conditions, power quality analysis, and power electronic applications.

Nicolás Toro-García: received the B.S. degree in electrical engineering and the Ph.D. degree in automatics from Universidad Nacional de Colombia, Manizales, in 1983 and 2012 respectively; the M.S. degree in production automatic systems from Universidad Tecnológica de Pereira, Colombia, in 2000. He is currently an Associate Professor in the Department of Electrical Engineering, Electronics, and Computer Science, Universidad Nacional de Colombia, sede de Manizales. His research interests include nonlinear dynamics of nonsmooth systems, and applications for switched inverters.

Fredy E. Hoyos-Velasco: received the B.S. degree in electrical engineering, the M.S. degree in automatics, and the Ph.D. degree in automatics from Universidad Nacional de Colombia, Manizales, Colombia, in 2006, 2009, and 2012, respectively. He is currently a Professor in the Department of Engineering, Tecnológico de Antioquia, Medellín. His research interests include nonlinear control, nonlinear dynamics of nonsmooth systems, and applications to dc–dc converters. He is a member of the research group Perception and Intelligent Control (PCI) and Ingeniería de Software from the Tecnológico de Antioquia (GIISTA).