

# Impact of Supply Voltage Distortion on the Harmonic Emission of Electronic Household Equipment

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**Abstract**— Electronic devices have a nonlinear characteristic and emit harmonics into the low voltage grid. Due to the mass-use of this equipment (consumer electronics, lamps with electronic ballast and so on) the harmonic levels in the grid are usually dominated by the emission of those devices. A lot of harmonic studies are available, which analyze their impact on the harmonic levels based on different types of harmonic models. One commonly used model is the constant current source.

Measurements have shown that the harmonic currents emitted by electronic devices significantly depend on the used circuit topology and the existing supply voltage distortion. The paper quantifies the impact of supply voltage distortion on the harmonic current emission of individual devices and the summation of multiple devices.

After a classification of the commonly used circuit topologies for each of them a model is developed. Based on a comprehensive simulation framework, the individual and combined impact of the most important voltage harmonics (3<sup>rd</sup>, 5<sup>th</sup>, 7<sup>th</sup>) on the harmonic current emission of the modeled devices is analyzed by a probabilistic study. Based on the results the accuracy of constant current source models is evaluated. Finally the impact of voltage distortion on the summation of multiple devices is analyzed and the accuracy of summation studies based on the measurements of individual equipment is assessed.

**Index Terms**— Power Quality, nonlinear loads, harmonics, attenuation effect, cancellation effect, diversity factors.

## ABBREVIATIONS

SMPS - Single-phase switch mode power supply  
PFC – Power Factor Correction  
CFL – Compact Fluorescent Lamp  
LED – Light Emitting Diode Lamp

## I. INTRODUCTION

THE amount of electronic devices used by residential, commercial and industrial users increase continuously. These devices are nonlinear loads that inject harmonic currents into low voltage grids, which could produce different problems, like unacceptable voltage distortion levels,

destruction of power-factor capacitors and the malfunction of equipment.

Most of the studies which analyze the impact of these technologies on the power quality are based on simulations which use an ideal current source to represent these loads (e.g. [1-2]). The parameters of the current source (magnitude and angle of the current harmonics) are usually obtained from measurements of the respective devices based on the specifications of international standards, like IEC 61000-3-2 [3]. These standards define a nearly undistorted voltage for the verification of current harmonics.

However, in the low voltage grids the voltage distortion is much greater, usually with THD values between 3% and 5% which change continuously during the day. This voltage distortion affects the current harmonics emitted by the electronic loads. Depending on the voltage waveform characteristics (magnitude and phase angle of the harmonics), harmonic emission of electronic loads can increase or decrease [4-6]. Therefore the current source may not be an adequate model for these kinds of loads.

The main aim of this paper is to analyze the effect of supply voltage distortion on the harmonic emissions of the main household electronic devices and to determine the usefulness of a current source to model non-linear loads. In the first part the time-domain models of generic electronic devices are developed. The generic models correspond to SMPS without

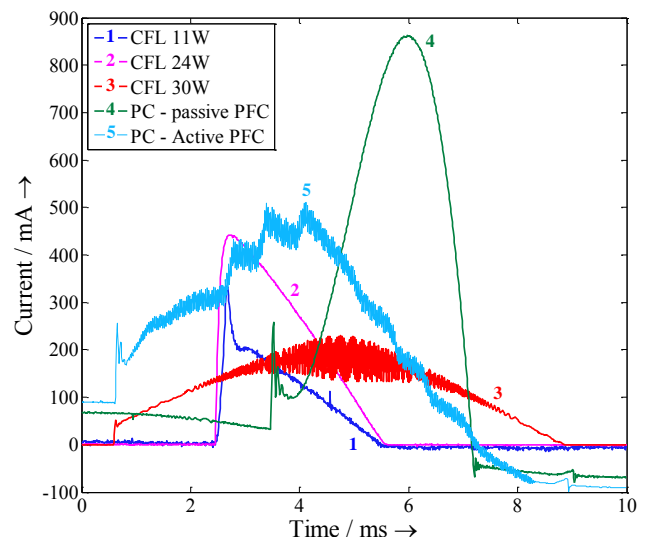


Fig. 1. Current waveforms of electronic devices with different circuit topologies (measurements with undistorted supply voltage)

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PFC, with passive PFC and with active PFC, which are the main electronic topologies available in the market [7].

In the second part the models were used to make several simulations in order to analyze the variation of the current harmonics emitted by single electronic devices when the magnitudes and angles of the voltage harmonics change. Finally, the results of simulations of mixtures of loads with distorted and undistorted voltage supply are analyzed to determine the impact on the cancellation effect.

## II. OVERVIEW OF ELECTRONIC LOADS

The electronic loads available in the market have different circuit topologies which lead to different current waveforms. Fig. 1 shows some typical current waveforms of different electronic devices.

Electronic devices usually have a SMPS. Simple SMPS without PFC have a two stage topology, consisting of rectifying and inverting stages. Rectifying stage includes capacitor-fed diode bridge rectifier and provides smoothed DC voltage to inverter stage which converts this DC voltage to a stabilized voltage/current signal of certain shape and level required by the load. Examples of this kind of load are the CFLs with rated power below 25W (see Fig. 1).

Depending on the existence of standardized limits (e.g. IEC 61000-3-2 [3]) some devices also implement a PFC. PFC methods can be classified as passive and active according to the utilized components. Passive PFC methods imply adding components like capacitors or inductors either to the input or the output of rectifying stage or using a valley-fill circuit in order to improve the shape of the current pulse. Being a cost-effective and reliable way to lower current distortion, passive PFC methods nevertheless increase the size and weight parameters of SMPS by using bulky capacitors and inductors as low frequency filters. These drawbacks are not present in active PFC topologies, utilizing various DC-DC converters (boost, flyback, SEPIC) that shape the input current waveform by HF-switching and control circuit.

Fig. 1 compares the current waveforms of electronic loads without PFC (CFLs <25W), with active PFC (CFL of 30W and one desktop computer) and passive PFC. Table 1 contains some characteristics of the devices obtained when an undistorted voltage waveform was used for the measurements.

TABLE I  
CHARACTERISTICS OF SOME ELECTRONIC LOADS MEASURED WITH AN UNDISTORTED VOLTAGE WAVEFORM

	$P$ [W]	$I_{rms}$ [mA]	$PF$	$THD_i$ [%]
CFL 11W (no PFC)	10,66	80,7	0,57	107,6
CFL 24W (no PFC)	22,08	156,8	0,61	109,5
CFL 30W (active PFC)	27,36	121,6	0,97	15,27
PC active PFC	48,09	258,3	0,80	30,24
PC passive PFC	55,78	340,1	0,71	100,07

Active PFC topologies have lowest distortion and a best power factor; however the almost sinusoidal waveform is superimposed with a higher frequency component. This higher frequency emission can also cause considerable network disturbances, but is not in the focus of this paper.

## III. MODELING OF ELECTRONIC LOADS

In order to analyze the effect of voltage distortion on the harmonic emission of electronic devices, the three different topologies were simulated in the Time-Domain. The Time-Domain modeling was selected because it allows a most detailed modeling of the device behavior in terms of harmonic emission. The models were designed to accurately represent the low-order harmonic emissions. As mentioned above, the higher frequency components are neglected for this analysis. Each topology was simulated in *Matlab*® with the *Simulink*® package. To verify the models several measurements with random voltage waveforms were made.

### A. SMPS without PFC

The simulated circuit is shown in Fig. 2a. The rectifying stage has a resistor ( $R_s$ ) to limit the current peak, a full diode bridge and a smoothing capacitor ( $C_p$ ). The inverting stage has only a resistance ( $R_L$ ) which represents the resonant inverter and the load (the tube in case of CFLs). This simplification does not affect the harmonic analysis because the resonant inverter normally runs at 10 – 40 kHz and this appears as a constant load from the source [8-9].

The values of resistance  $R_L$  and the capacitance  $C_p$  depend on the active power of the lamp, while  $R_s$  is fixed to about 10Ω. The value of  $R_L$  decreases and the value of  $C_p$  increases with the power of the lamp. Several ways exist to determine the

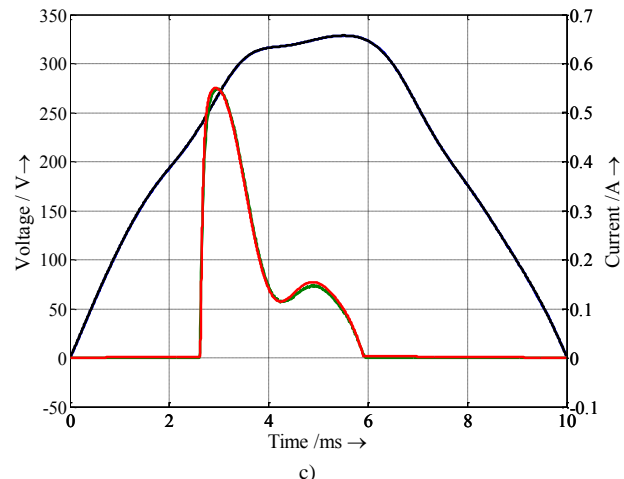
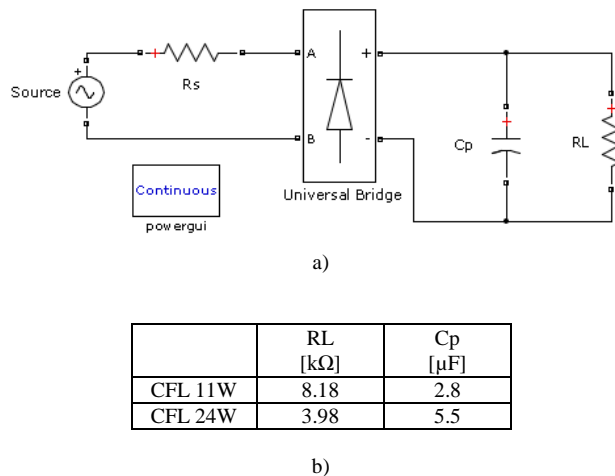


Fig. 2. SMPS without PFC. a) Circuit topology, b) Parameters for two CFLs of 11 and 24W, c) Simulated (red) and measured (green) current waveforms of a 24W CFL for a particular voltage distortion.

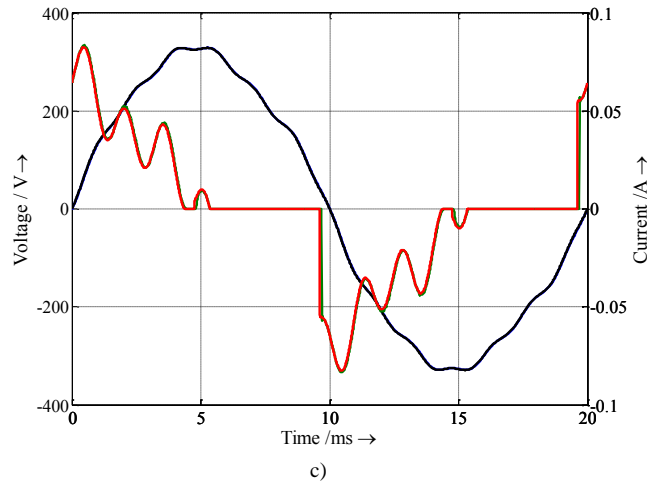
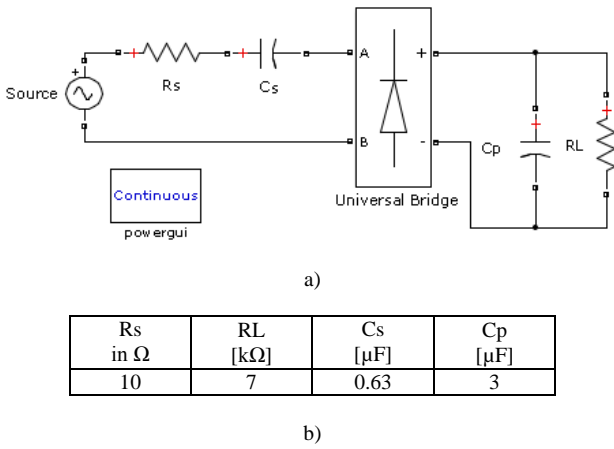


Fig. 3. SMPS with passive PFC. Topology with a series capacitor (LED 3.5W). a) Circuit topology, b) Circuit parameters, c) Simulated (red) and measured (green) current waveform for a particular voltage distortion.

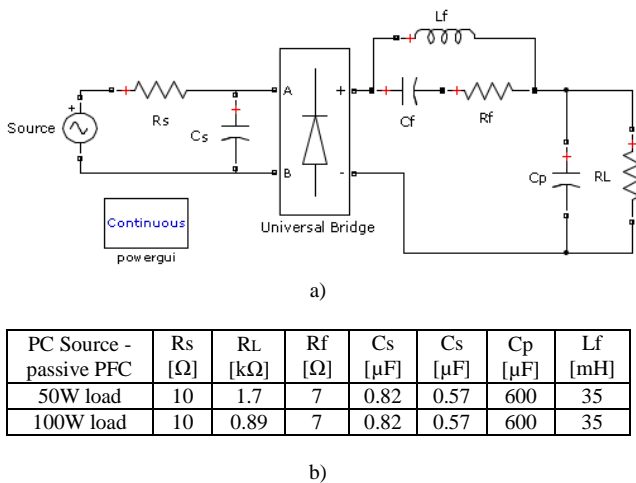
value of  $R_L$ . More information can be found e.g. in [7]. The value of  $C_p$  is found using an iterative process until the error between the measured values and the simulations reaches a minimum. The values of  $R_L$  and  $C_p$  for two selected CFLs of 11W and 24W are presented in Fig. 2b.

The model was verified using measurements of both lamps under different voltage distortions. Fig. 2c shows the voltage and current waveforms of the 24W CFL obtained in one measurement (green curve) and the corresponding simulation (red curve). As can be seen, the simulation represents properly the current waveform of the lamp.

### B. Passive PFC

There are different ways to improve the power factor using passive elements, so there is not a unique configuration that can represent these kinds of devices. Reference [10] presents a survey of most popular passive PFC methods, showing their great topological diversity. For this study only two configurations were implemented corresponding to a LED lamp and a PC source.

Fig. 3a shows the simulated circuit of a LED lamp of 3.5W.



In this case only a capacitor was added to the simple configuration of a SMPS (Fig. 2a). The parameters for this model defined according to [11] are shown in Fig. 3b. Comparison of simulated and measured current waveforms in Fig. 3c shows good matching of model and experiments.

Unlike LEDs, PCs with passive PFC tend to have one common circuit consisting of capacitor-filtered diode bridge rectifier and smoothing inductor acting as a passive harmonic filter. The inductor widens the current pulse thus improving its distortion. Depending on usage behavior, the power consumption of a PC can vary in large ranges. To include this in the analysis, 2 load levels (50W and 100W) are considered. The first corresponds to normal mode of editing documents or browsing the internet, the second is dedicated to more power consuming applications, like games or video rendering [12]. The topology of PC power supply under study is shown in Fig. 4a.

Input current waveform of considered PC power supply presents a step at the beginning of the conduction interval due to parallel resonant circuit ( $C_f$  and  $L_f$ ), that is used to widen

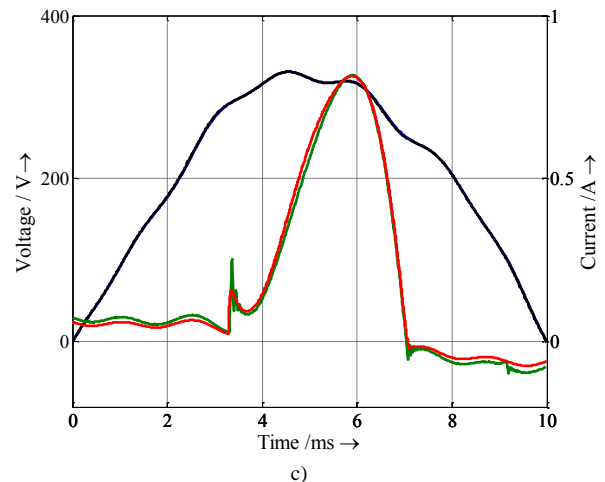


Fig. 4. SMPS with passive PFC. Topology with smoothing inductor (e.g. some PC power supplies). a) Circuit topology, b) Circuit parameters, c) Simulated (red) and measured (green) current waveform for a particular voltage distortion.

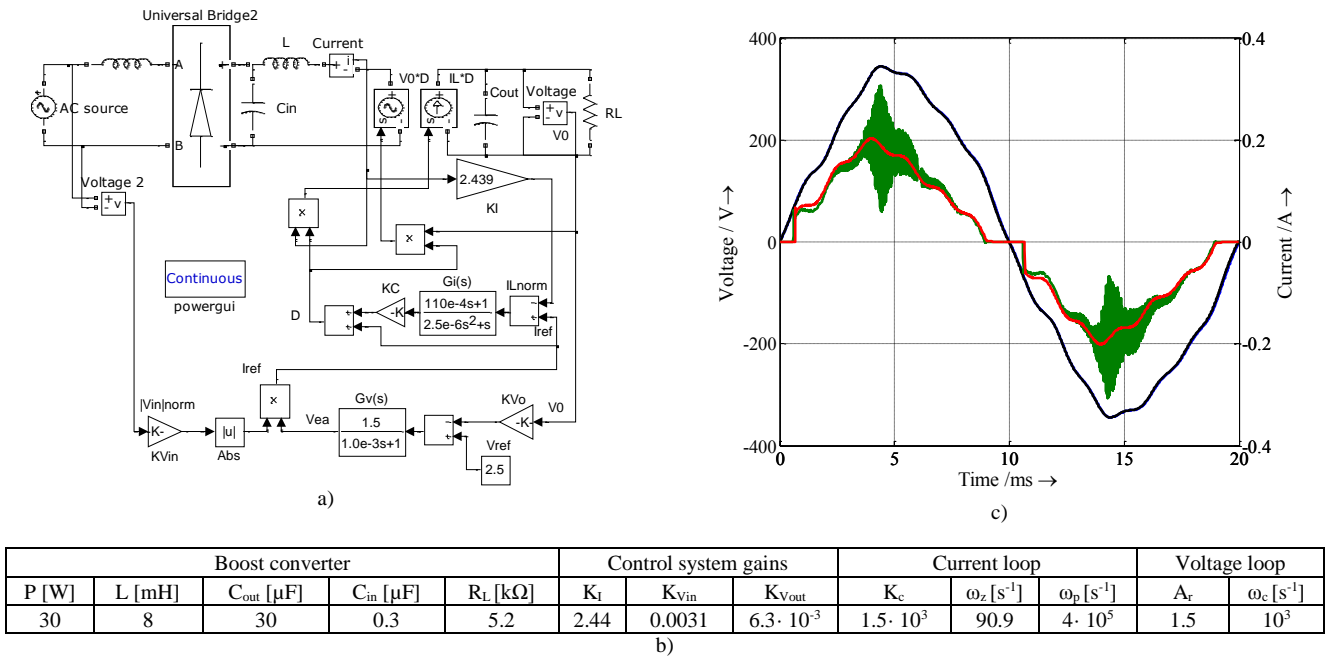


Fig. 5. SMPS with active PFC (30W CFL). a) Circuit topology, b) Circuit parameters, c) Simulated (red) and measured (green) current waveform for a particular voltage distortion.

current pulse at higher loads. Moreover current waveform of Fig. 4c is non-zero when diodes are reverse biased because of the presence of EMI filtering small capacitor  $C_s$ . The values of the model parameters for two load states are depicted in Fig. 4b.

Superimposing simulated and experimental waveforms proves good quality of developed model for PC power supply with passive PFC.

### C. Active PFC

The general idea of active PFC methods implies shaping the input current to resemble the waveform of the sinusoidal line voltage by means of HF switching of boost DC-DC converter. Nevertheless, there is a certain level of current distortion inherent for all active PFC circuits [13] that involve zero-crossing distortion and nonsinusoidal shaping of the current waveform. It can be claimed that control system of active PFC circuits defines on the whole its current harmonic spectrum.

In terms of the present paper only an active PFC circuit of 30W CFL was considered. Active PFC topology utilized in 30W CFL consists of diode bridge rectifier, boost converter and control circuit made up of voltage and current control loops (Fig. 5a).

To simplify and speed up simulation the operation of boost DC-DC converter was modeled via averaging approach. HF switching was neglected and transistor and diode were replaced with so called “DC transformer”, involving voltage and current sources, subsequently,  $V_0 \cdot D$  and  $I_L \cdot D$ , controlled by duty cycle  $D$ . Voltage control stabilizes the output voltage by means of transfer function  $G_V(s)$ :

$$G_V(s) = A_r / (s/\omega_c + 1) \quad (1)$$

where  $A_r$  is the low frequency gain of the voltage controller and  $\omega_c = 2\pi f_c$  the corner frequency in rad/sec.

Current shaping is guaranteed by current control loop that compares the reference signal from voltage loop  $I_{ref}$  with inductor current with the following transfer function  $G_I(s)$ :

$$G_I(s) = \frac{K_c(s/\omega_z + 1)}{s(s/\omega_p + 1)} \quad (2)$$

where  $K_c$  is the integrator gain and  $\omega_p$  and  $\omega_z$  are the HF pole and zero of the transfer function.

Parameter calculation procedures for boost converter, voltage and current control loops (Fig. 5b) are provided by [14].

Comparison of simulated and measured current waveforms for active PFC 30W CFL presented in Fig. 5c shows that modeled curve follows closely the average measured waveform. As already mentioned the models are focused on low order harmonic emission and therefore higher frequency emission is not reflected by the model.

## IV. ANALYSIS OF INDIVIDUAL ELECTRONIC DEVICES

The effect of supply voltage distortion on the current harmonic emission of the major circuit topologies is analyzed with the models developed in Simulink. The model of the 24W CFL, the PC source (50W load) and the 30W CFL were selected for the simulations because they represent the main circuit topologies, namely the SMPS without PFC, the SMPS with passive PFC and the SMPS with active PFC respectively.

### A. General Framework

As a first step this study limits the analysis to the effect of the 3<sup>rd</sup>, 5<sup>th</sup> and 7<sup>th</sup> voltage harmonics only. These harmonics represent the dominating harmonic orders in most of the low voltage grids. Ten cases with different variations of these voltage harmonics were defined (see Table II). The first 6 cases consider the effect of each voltage harmonic individually,

when the magnitude changes between 0 and 4% and the angle varies between 0 and 90° or between 0 and 360°. The other cases consider the effect of two or three voltage harmonics at the same time. As reference the measurement with undistorted voltage is used.

TABLE II  
DEFINED CASES FOR THE ANALYSIS

Case	Voltage harmonics ( $V^{(h)} \angle \theta^{(h)}$ )					
	$V^{(3)}$ [%]	$\theta^{(3)}$ [°]	$V^{(5)}$ [%]	$\theta^{(5)}$ [°]	$V^{(7)}$ [%]	$\theta^{(7)}$ [°]
1	0-4	0-90	-	-	-	-
2	0-4	0-360	-	-	-	-
3	-	-	0-4	0-90	-	-
4	-	-	0-4	0-360	-	-
5	-	-	-	-	0-4	0-90
6	-	-	-	-	0-4	0-360
7	0-4	0-360	0-4	0-360	-	-
8	0-4	0-360	-	-	0-4	0-360
9	-	-	0-4	0-360	0-4	0-360
10	0-4	0-360	0-4	0-360	0-4	0-360
Ref.	0	-	0	-	0	-

Sets of 300 different voltage waveforms were generated for each case. Therefore magnitudes and angles of the voltage harmonics are drawn from uniform distributions and within the ranges given in Table II. As an example, Fig. 6 shows the cumulative distribution of the 5<sup>th</sup> harmonic magnitudes and angles of the voltage waveforms sampled for case 4. To ensure comparability each device was simulated for each case with the

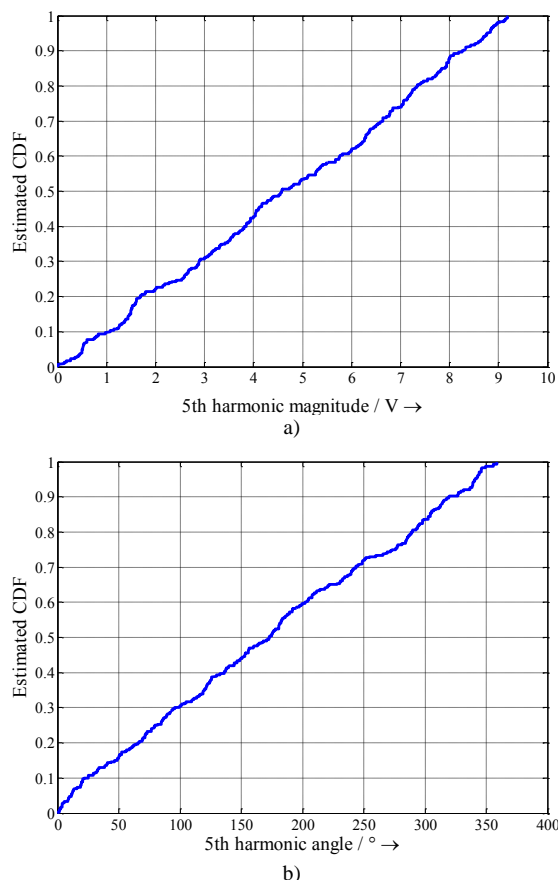


Fig. 6. CDF of 5<sup>th</sup> harmonic of voltage waveforms generated for case 4.  
a) Magnitudes, b) Angles

same set of voltage waveforms and the THDi and the first odd current harmonics were recorded. Fig. 7a exemplarily shows the cumulative distribution of 5<sup>th</sup> harmonic current magnitude that is obtained for case 4. It can be seen that the uniformly distributed 5<sup>th</sup> harmonic voltage magnitudes and angles result in a distribution of 5<sup>th</sup> harmonic current magnitude that is unsymmetrical and non-uniform.

For further analysis the difference between simulation results and reference case (marked by a red dot in Fig. 7a) is calculated in order to represent the impact of voltage distortion clearly and to compare the results of the different topologies. Fig. 7b exemplarily shows the distribution function of this difference. Selected numbers are given in Table III. Finally, the 5<sup>th</sup> to 95<sup>th</sup> percentile range is obtained for each data set to quantify the variation of the THDi and the current harmonics by respective boxes (c.f. Fig. 7b).

It has to be noted, that absolute difference and difference related to fundamental lead to different interpretations. Both have advantages and disadvantages. Refer to next subchapter for more details.

TABLE III  
REFERENCE VALUES

Device	THDi (%)	Current harmonics ( $I^{(h)} \angle \theta^{(h)}$ )			
		$I^{(1)}$ [mA]	$\theta^{(1)}$ [°]	$I^{(5)}$ [mA]	$\theta^{(5)}$ [°]
No PFC	108.6	102.3	25.09	53.2	137.08
Passive PFC	91.9	236.3	357.07	105.2	285.41
Active PFC	14.5	117.7	10.40	6.4	233.03

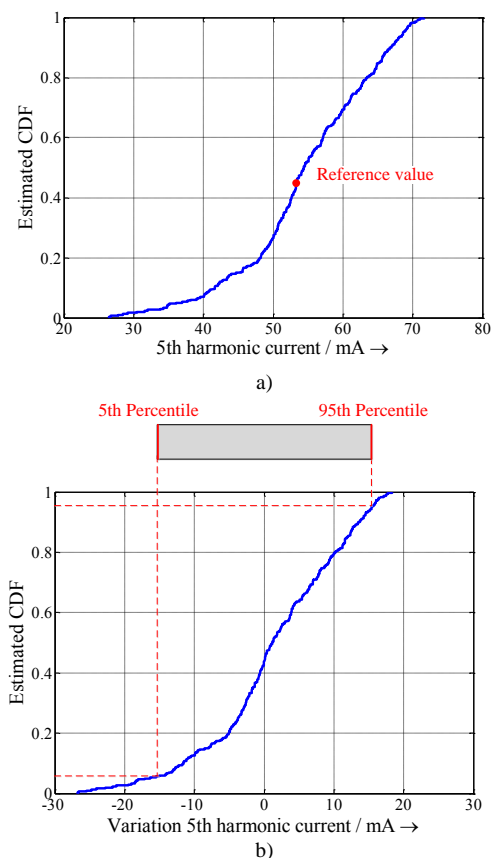


Fig. 7. Simulation results CFL 24W with Case 4. a) CDF 5<sup>th</sup> harmonic current, b) CDF Variation 5<sup>th</sup> harmonic current.

### B. Analysis of THD

The total harmonic distortion  $THD_I$  applied in this paper is defined as:

$$THD_I = \frac{I_{HAR}}{I_{FUN}} = \frac{\sqrt{\sum_{h=2}^{50} (I^{(h)})^2}}{I^{(1)}} \cdot 100\% \quad (3)$$

where  $I^{(h)}$  are the magnitudes of the current harmonics,  $I_{HAR}$  is the total rms harmonic current and  $I_{FUN}$  the rms fundamental current.

Fig. 8 shows the variation of the  $THD_I$  for the different cases. The  $THD_I$  varies for all the topologies. The variation increases for cases with higher voltage distortion. Moreover the  $THD_I$  variation is larger, if the voltage harmonic angles vary in a larger range ( $0^\circ \dots 360^\circ$  compared to  $0^\circ \dots 90^\circ$ ). This shows clearly the significant effect of voltage harmonic angles on the harmonic emission of electronic devices.

Between the topologies, the SMPS without PFC is more sensitive to the voltage distortion than the other topologies. The  $THD_I$  of this topology varies in the range of 12% to 40%, the current distortion of the SMPS with passive PFC in the range of 5% to 25% and the active PFC device in the range 1% to 5%. The topology without PFC behaves most sensitive while the active PFC seems to be the most robust topology in terms of supply voltage distortion.

The  $THD_I$  is related to the fundamental and provides a good index for comparing the sensitivity between the different equipment. However the  $THD_I$  may not only result from variation of harmonic currents but also from variation of fundamental current. To avoid any misinterpretation, Fig. 9 presents the variation of total harmonic current  $I_{HAR}$  and fundamental current  $I_{FUN}$  separately. It shows that the fundamental current of passive PFC device is much higher affected by the different voltage distortions than for the other equipment, while the fundamental current for active PFC device is almost independent from it. The total harmonic current of the passive PFC device has the highest variation, which is at least partly caused by its higher absolute current emission compared to the other devices. Moreover in case of the limited phase angle variation of 3<sup>rd</sup> harmonic voltage

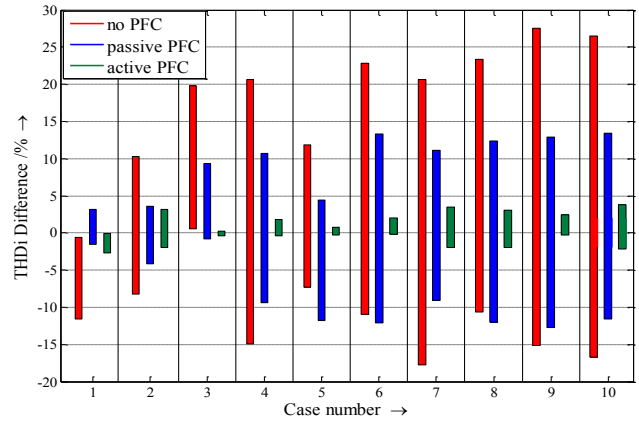


Fig. 8. Variation of the  $THD_I$  of main topologies due voltage distortion.

(case 1) fundamental current and total harmonic current decrease, while similar variation of 5<sup>th</sup> harmonic voltage (case 3) shows opposite behavior. Reason for this is the different impact of both voltage harmonic variations to the voltage waveform. While a 3<sup>rd</sup> harmonic voltage with phase angles in the range  $0^\circ \dots 90^\circ$  tends to flatten the voltage waveform, similar phase angle variation of the 5<sup>th</sup> harmonic voltage results usually in pointed top waveforms. This impact e.g. cannot be derived from the  $THD_I$  variation in Fig. 8.

### C. Analysis of harmonic emission

The impact of voltage distortion on the individual harmonics is exemplarily discussed for the 5<sup>th</sup> harmonic current. Due to its dominance, the behavior of 5<sup>th</sup> harmonic currents in Fig. 10a) is almost similar to that of the total harmonic current in Fig. 9 b). According to Fig. 10 b) the phase angle variation has highest values for the active PFC device, while the devices without PFC and with passive PFC behave almost similar and show lower variation range. This is in contrast to the behavior of the magnitude changes. Generally there is no linear link between variation of voltage harmonic phase angle and current harmonic phase angle.

Another interesting aspect is the cross-interference between the harmonics. A zero cross-interference means that the n<sup>th</sup> harmonic voltage will only result in a n<sup>th</sup> harmonic current. All other harmonic currents are not affected [5]. Consequently

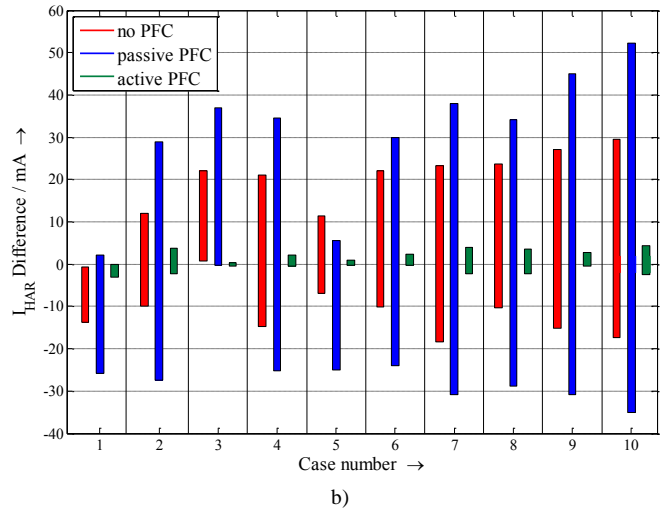
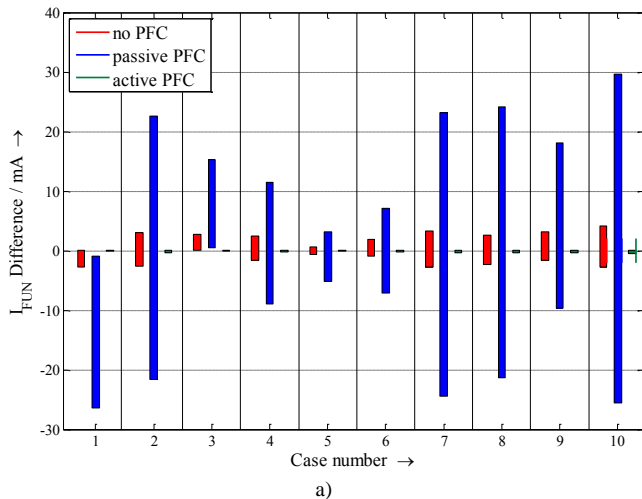


Fig. 9. a) Variation of the rms fundamental current and b) variation of the total harmonic current of main electronic topologies.

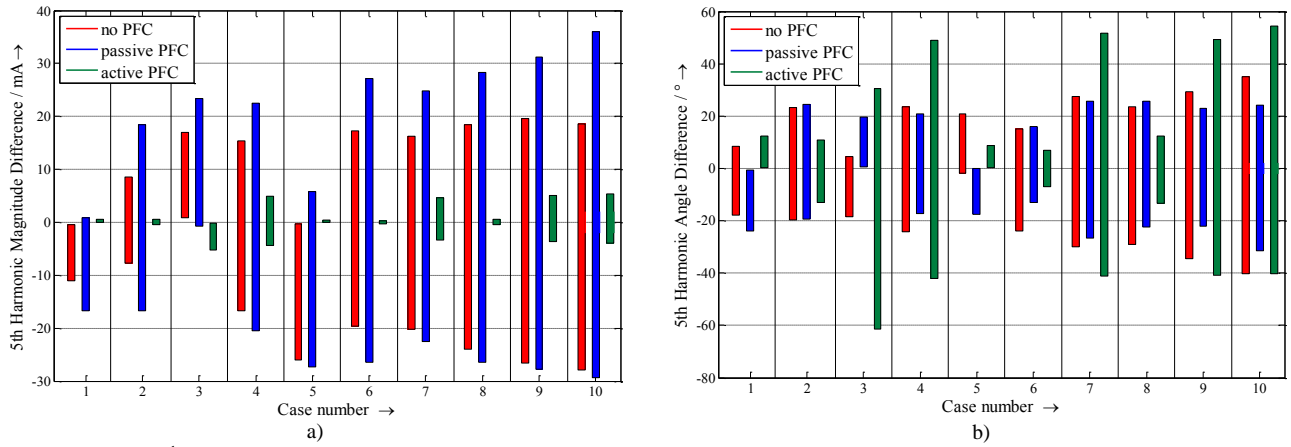


Fig 10. Variation of the 5<sup>th</sup> current harmonic due voltage distortion. a) Magnitudes, b) Angles

Fig. 10 would show harmonic current variation only for the cases 3, 4, 7, 9 and 10. However, this is only satisfied for the harmonic current magnitudes of the active PFC device, which mainly results from the internal PFC control of the device. The simple SMPS without PFC as well as the passive PFC device show a significant cross interference, which complicates the development of accurate but simple models further.

#### D. Summary

With these results it is clear that the traditional modeling of electronic devices with a constant current source may result in significant inaccuracies in the frequency domain. The current harmonic emission depends on the voltage harmonics magnitudes and angles. Most dependencies are not linear. All topologies show more or less distinctive cross-interference, which means that independent consideration of harmonic orders and superposition are only limited applicable.

If a quick harmonic study is needed, current source models may be sufficient. However depending on the particular situation in terms of voltage distortion significant errors of several ten percent have to be expected. For accurate and reliable analysis it is better to use the time domain models.

#### V. ANALYSIS OF A GROUP OF ELECTRONIC DEVICES

The presence of different devices with different topologies at one connection point can cause a diversity of current

harmonic phase angles and subsequently may lead to a lower magnitude of vector sum than the arithmetical sum of the harmonic currents [9, 15]. This is known as cancellation effect and has a high influence on the total harmonic distortion emitted by larger groups of electronic devices into the grid.

The cancellation effect is quantified by the phase angle diversity factor  $k_p^{(h)}$  individual for each harmonic [16]:

$$k_p^{(h)} = \frac{\text{Vector sum}}{\text{Arithmetic sum}} = \frac{I_{VEC}^{(h)}}{I_{ARI}^{(h)}} = \frac{\left| \sum_{i=1}^n I_i^{(h)} \right|}{\sum_{i=1}^n |I_i^{(h)}|} \quad (6)$$

where  $I_i^{(h)}$  represents the harmonic current vector of the device  $i$ ,  $n$  is the number of devices and  $h$  is the order of the harmonic. The diversity factor varies between 0 (perfect cancellation) and 1 (no cancellation). This study shall give an idea on accuracy and representativeness of diversity factors calculated based on individual harmonic currents measured at a particular voltage distortion [e.g. 16].

To analyze the effect of voltage harmonics on the cancellation between individual harmonic currents within a group of electronic devices, the time domain models of two devices without PFC (CFLs with 11W and 24W), one passive PFC device (PC power supply at 50W) and one active PFC device (CFL with 30W) are together connected to the same

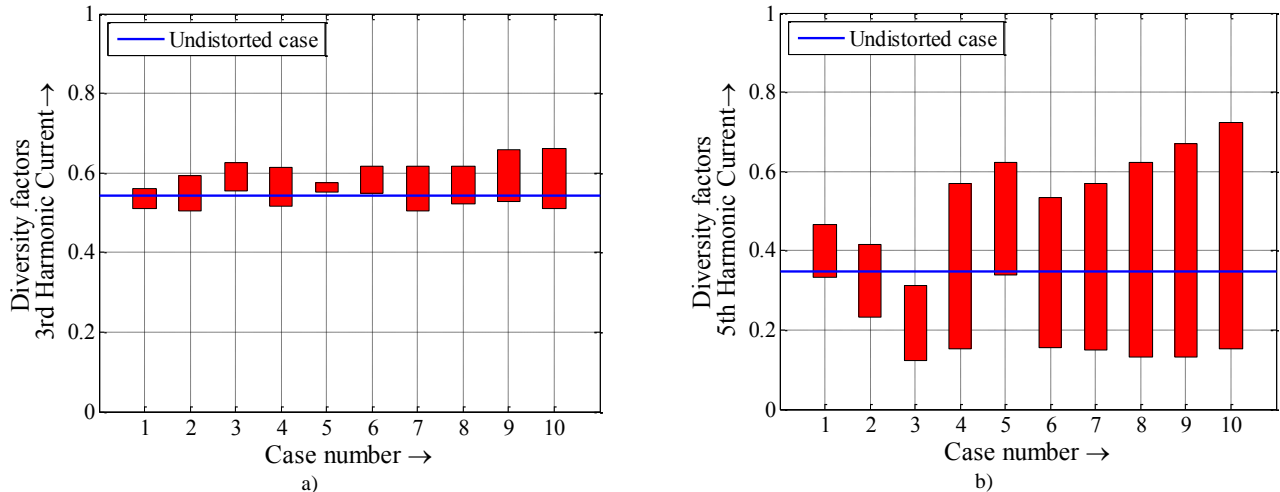


Fig. 11. Variation of phase angle diversity factors due to voltage distortion. a) 3<sup>rd</sup> harmonic current, b) 5<sup>th</sup> harmonic current.

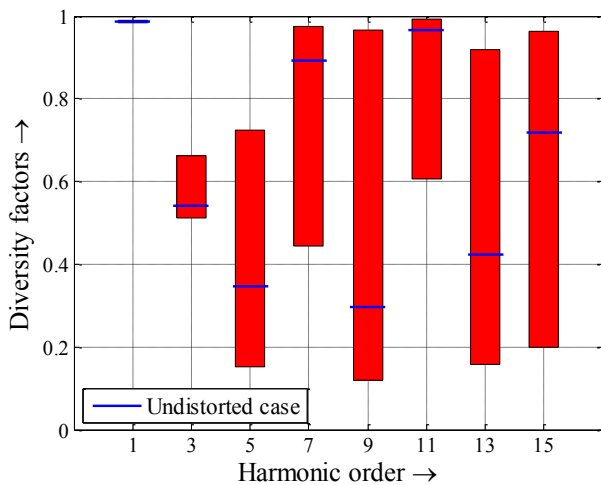


Fig 12. Variation of diversity factors for the first LV harmonics. Blue lines represent the diversity factors obtained with an undistorted voltage.

point. The diversity factor  $k_p^{(h)}$  is calculated for each case according to Table II using the same sets of randomly generated voltage distortions. Analog to chapter 4 the 5<sup>th</sup> to 95<sup>th</sup> percentile range is calculated and presented as a box. The reference case at undistorted supply voltage is indicated by a blue line.

Fig. 11 shows the variation of the diversity factor of the 3<sup>rd</sup> and 5<sup>th</sup> current harmonic for each of the cases. The diversity factor of the 3<sup>rd</sup> harmonic shows only a very low variation. In terms of 3<sup>rd</sup> harmonic the level of cancellation for a group of devices at a single connection point is almost independent from the voltage distortion. The diversity factor remains close to the one obtained at undistorted voltage.

For the 5<sup>th</sup> harmonic the variation is significant. Without voltage distortion the cancellation for the 5<sup>th</sup> harmonic current is very effective (0.35). In case of a 5<sup>th</sup> voltage harmonic varying in the range 0° ... 90° the efficiency increases, but for most of the other cases a partly decrease of the diversity can be observed. However a certain amount of cancellation always exists. Nevertheless an accurate and reliable study of cancellation effect for 5<sup>th</sup> harmonic current should take voltage distortion into account. This can be achieved e.g. by introducing probabilistic aspects to the device modeling.

The combination of the results of all 10 cases (3000 random voltage distortions) into one box for each odd harmonic up to 15<sup>th</sup> is presented in Fig. 12. The reference case (undistorted supply voltage) is indicated by the blue line. As expected the fundamental adds up arithmetically independent of voltage harmonics. For harmonic orders 7 and above the variation of diversity factor becomes very high. Even situations without any cancellation may occur. Therefore studies of the cancellation effect based on equipment measurements under undistorted supply voltage should be interpreted with care.

## VI. CONCLUSIONS

Electronic household devices can be divided into three main circuit topologies: SMPS without PFC, SMPS with passive PFC and SMPS with active PFC. All the topologies produce current harmonics which depend strongly on the distortion of the supply voltage.

The application of the current source model is limited and can result in errors of several ten percent if supply voltage is

distorted. The current emissions depend not only on the magnitude of the voltage harmonics, but also on the angles, and in most of the cases these relations are not linear. Most of the analyzed cases show a significant cross-interference. This means that changes in one voltage harmonic lead to changes in multiple current harmonics. Introducing probabilistic aspects into the current source model can improve the quality and reliability of results. For accurate harmonic studies the use of time domain models is highly recommended.

The cancellation effect of current harmonics of order 5 and higher is highly affected by the presence of voltage harmonics. Therefore the cancellation of current harmonics not only depends on the number and type of connected devices, but also on the voltage distortion in the low-voltage grid. Subsequently realistic harmonic studies on the impact of electronic mass market equipment on the harmonic studies should also take the voltage distortion into account.

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