SICEL VII Simposio Internacional sobre Calidad de la Energía Eléctrica 2013

Operation Strategies with Tolerance to Faults in Multilevel Inverters to Ensure Continuity Process in Industrial and Mining Systems

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***Abstract*— Industry and mining sectors use large engines driven by variable speed drives, which greatest fault rate is presented in multilevel inverter stage. This article shows operating strategies in tolerance to faults multilevel inverters, focusing on the reconfiguration of the modulation of trigger signals, in order to ensure continuity of service without affecting the operation of the motor.**

We present the strategy for NPC (Neutral Point Clamped) multilevel inverters of three levels and CHB (Cascaded H Bridge) of seven levels, simulating its action on an electric mining system, modeled in PSCAD / EMTDC software.

***Index Terms*— Multilevel Inverters, Tolerance to faults, IPDPWM Modulation, NPC inverters, CHB inverters.**

I. Introduction

IN INDUSTRY and mining we seek to optimize the process using variable speed drive in low and medium voltage, these have more interest from the point of view of continuity of service, and they handle higher power and they are neuralgic points for the production process .

Medium voltage variable speed drives (VSD) in inverter stage, present multilevel inverters (there are three basic types of multilevel converters: neutral point clamped (NPC) multilevel cascade (CHB) and flying capacitor (FC). Complete revision of multilevel inverters topologies MLM is shown in [1] and [2]. Articles have been written about these control systems and their functionalities of these inverters when they are part of the VSD [3] [4] [5] [6]. Commercially There are three and five levels and have written several articles explaining their characteristics and differences [7] [8] [9] [10] [11].

For own freaks of VSD or network occur faults in the inverter stage in their switching devices (can be basically of two types, fault mode to open circuit and fault mode to short circuit), these faults can affect the behavior of engines and even produce a total halt production. When this happens, the process has considerable economic losses. Many times there are no switching devices to replace them and you have to import the components which shipping times in most cases are more than two months. Because the consequences of fault, various equipment redundancy strategies (use of extra components) have been presented as fault tolerant systems. [12] [13] [14].

This paper shows a strategy for the control system of the switching devices in inverter stage can be reconfigured the trigger signals in order that the VSD can tolerate the faults without affecting the operation of the engine, as the applied voltages will be balanced and in some cases without changing the amplitude.

One advantage of this strategy is that no additional components are used to tolerate faults, everything is done to control levels, as shown in [15] [16] [17].

Strategy is presented for three-level NPC inverters and seven-level CHB, simulating its action on an electrical subsystem great Peru mining, modeled in PSCAD / EMTDC software.

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II. Objective

- Model and simulate a control system that allows multilevel inverters can tolerate faults produced in the switching devices, by reconfiguring the modulation of trigger signals.
- Model an existing system and test the proposed strategy by simulating and explaining the results.

III. Fault Modes of Multilevel Inverters

In [18] we speak of the faults produced in inverters classifying: in: faults in diodes of rectification stage, faults in power electronic devices (DSEP), fault in control stage, thermal faults in the DSEP and faults from the load.

The most common faults in the DSEP are:

- Open circuit devices 18%
- Short circuit devices 15%
- Faults in the control 30%
- Faults by thermal fatigue 25%
- Other faults 12%

The faults in the short circuit devices and open circuit represent 33% of faults that can occur, the thermal and control faults depend on constructive aspects, this article is aimed to provide a fault tolerant system so we will put more emphasis on the first two types of fault.

A. *Fault Mode to Open Circuit*

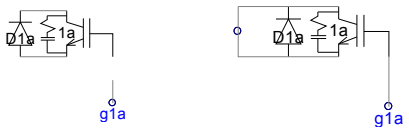
It comes in the switching devices when one of them is off even when the trigger signal is activating. When this happens it is not possible to transfer power to the load.

Fault of this type may have various origins; it can be a problem on the component for thermal causes, contact wear, among others.

B. *Fault Mode to Short Circuit*

It occurs when a driver is closed while the other closed in the same branch of the inverter cell when this fault occurs it is not possible to transfer power to the load, so that an overcurrent occurs between the supply voltage and two DSEP.

Fig.1 b) shows a simplified circuit representative of this type of fault.



a) b)

Fig. 1. Simplified circuit: a) Fault Mode to Open Circuit b) Fault Mode to Short Circuit

IV. Fault Detection in Invertors Multiswitch

Here are some important techniques to detect and locate faults in the DSEP. These techniques can be divided into four groups:

A. *Current Trajectories*

This technique begins of the DSEP behavior when it is connected to an induction motor. For example if it were an open circuit fault, the current of Fig.2 leaves to be sinusoidal. This fault cancels the current in the damaged phase for some time. The technique to detect and localize the fault is done by monitoring the current paths using Clark transform.

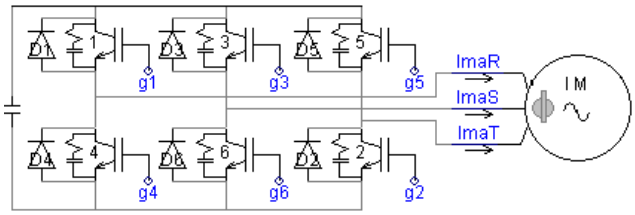


Fig. 2. Simplified Diagram: Inverter – Engine

It is important stand out that you need at least ½ cycle to detect the damaged phase, this technique does not apply to the fault mode in short circuit, and the estimated time of fault location grows for the computation time that involves the Clark transform and the sampling time of the digital processing system. The greatest condition of danger is provided by the device in short circuit.

B. *Vector Composition of the Voltage Harmonics*

This technique is based on the characteristics of the output waveform, particularly significant component of the switching frequency when a fault by fault mode in short circuit. The detection technique is to measure the magnitude of the component and comparing it with a threshold level, for determining the location of the damaged element is used the existence of offset of internal voltage phases for each branch or cell.

C. *Measuring of Voltage in Inverter Poles*

This technique is based on the effect that causes a breakdown by mode of open circuit fault in an error signal, which is obtained by comparing the pole voltage (medium voltage of branch) and the pattern reference voltage PWM. This difference must be confirmed in approximately 4ms, these errors can be positive or negative, it is important calibrate properly the data acquisition module.

D. *Inverter Switching times*

This technique is based on the basis of the method "actuator as sensor", the voltage between the terminals of DSEP is used as a sensing element. The fault diagnosis is performed by observing signals on characteristics of steady state of DSEP. It also complements an analysis using the system model for better troubleshooting. To avoid false alarms, it is required that each commutation is evaluated twice, therefore proposes an overlapping time of switching either power on or power off.

V. Operating Strategies with Tolerance to Faults in Multilevel Inverters with Material Redundancy

The effort to give reliability to the system seeking that multilevel inverters can withstand the fault it is given since 2004. [12] [13] [14] [15].

Welchko [19] performes a comparison of fault-tolerant topologies in inverters with material redundancy, as redundancy with a switch, two switches and additional branch all of them use as reference the topology shown in Fig 2.

A. *Tolerance to Fault with Power Switch*

Fig.3a shows the topology used in this scheme that incorporates four triacs and three fast acting fuses, the fuses are connected in series with the load phases.

B. *Tolerance to Fault with two Power Switches*

Fig.3b shows the topology used, it consists of four branches within the inverter, with additional components (two fuses and two SCR for each branch, and two capacitors)

C. *Tolerance to Fault with Additional branch*

Fig.3c shows the topology employed, it consists of four branches within the inverter, this topology unlike the previous two does not require to split to the dc source.

VI. Operating Strategies with Tolerance to Faults in Multilevel Inverters with Reconfiguration of Activation Signals NPC-3 Levels

The technique is not based on physical replacement of components, is based on changing the modulation signals in this case is a variation of the carrier signal using the technique IPDPWM. As the inverter is a three-level NPC and we wish to

preserve the position of the components, we will analyze the system from the fault of a switching device.

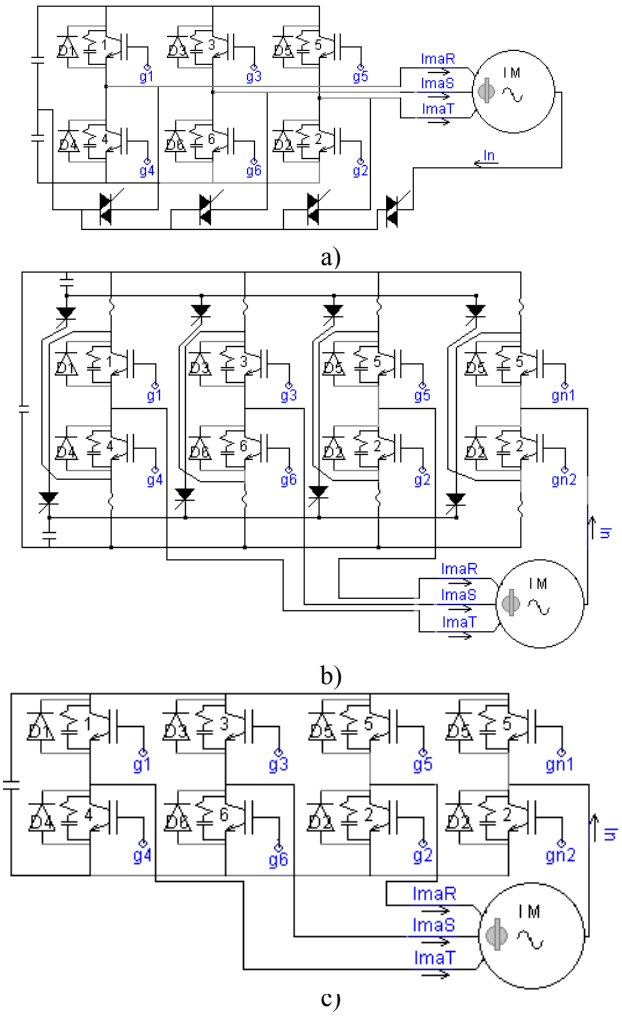


Fig. 3. Operation Strategies with Material: Redundancy a) With a switch, b) With two switches, c) With Additional Branch

A. System Analysis

Figure 4a shows the system when a component fails. The proposed system is based on the work developed in [20], which raises the possibility that the engine can operate at lower voltage levels and it is made inclusive an experimental development. This makes the strategy from vector diagrams.

In this paper, we allow the system to operate in the conditions described by Shengming, but modifying the trigger signals on the modulation technique IPDPWM. The fault could occur at any stage in the diodes and IGBTs either in open mode or short circuit. Here we analyze the short-circuit mode, as the one that best presents. If we consider the phase A, we have three cases:

- Case 1: T11 or T14 in short circuit.
- Case 2:T12 or T13 in short circuit.
- Case 3: D1R or D2R in short circuit.

Under any of these conditions we arise to join phase A to the junction point of the capacitors, as shown in Fig 4b. This does not involve removing the IGBTs of phase A, but in modulation level stop switching them. Another way is to send a control signal to a bypass switch to join stage A with point Z.

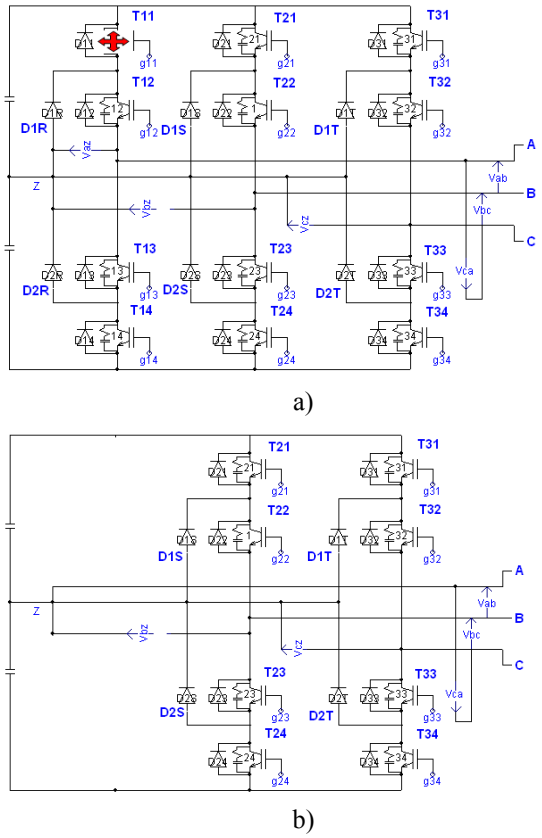


Fig. 4. Operation Strategies with Reconfiguration of Activation Signal NPC-3 levels: a) Fault in phase A, b) Inhibit Phase A.

B. Changing of Activation Signals

This technique of reconfiguration takes into account IPDPWM modulation, assigning two carriers in phase at different voltage levels and comparing it with a reference signal, thereby obtaining trigger signals for the IGBTs, as shown in Fig 5.

When fault occurs you have to isolate or stop switching the phase with fault. The other phases have to be modified for the engine to operate at lower voltage because of this the reference signals for the other phases also will change as shown in Table I.

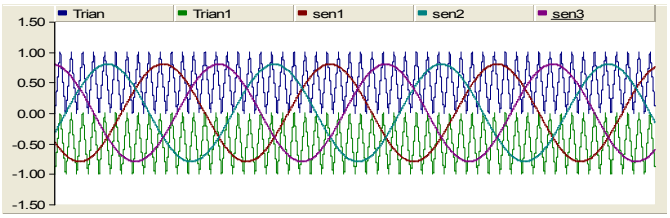


Fig. 5. IPDPWM Modulation-NPC-Three Levels

TABLE I
REFERENCE SIGNALS

$V_m a(\omega t)$	$V_m b(\omega t)$	$V_m c(\omega t)$
0	$\frac{2}{3}M.sen(\omega t+\pi/2)$	$\frac{2}{3}M.sen(\omega t+5\pi/6)$

C. Control System and Dynamic Response System

As indicated in Table I, the modulating signals are changed for each phase in order to have a balanced line voltage

Fig 6 shows the new reference signals, the voltages and currents in the engine.

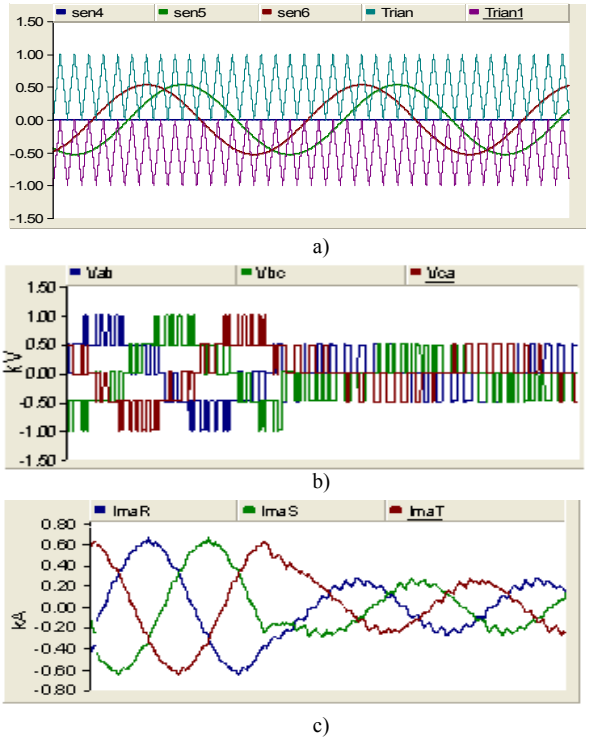


Fig. 6. System Response a) Reference signals, b) Voltages in the engine, c) Current in the engine

VII. Operating Strategies with Tolerance to Faults in Multilevel Inverters with Reconfiguration of Activation Signals CHB-7 Levels

The technique relies on changing the modulation signals, following the technique IPDPWM. Here we will discuss two possible cases, to fail a cell or to fail two cells.

A. Fault in a switching device

Fig. 7 represents the system when one component of the first cell fails. The fault could occur at any part of the cell, in the diodes or IGBTs either in open circuit mode or short circuit.

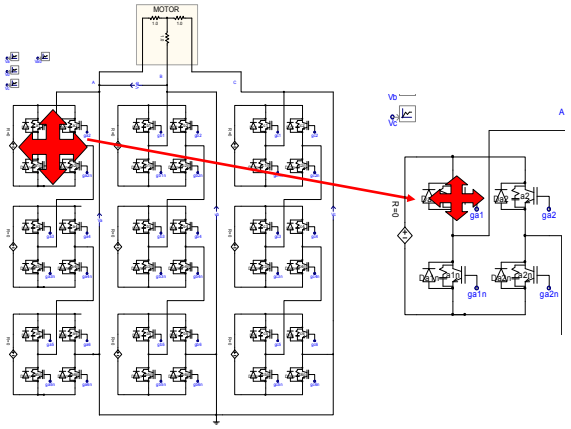


Fig. 7. Fault in a Switching Device.

This reconfiguration technique takes into account IPDPWM modulation, assigning six carriers in phase to different voltage levels and comparing it with a reference signal, thereby obtaining trigger signals for the IGBTs. Fig.8 shows how signals are distributed in each cell per phase.

We analyze the modulation index and the reference signal changes in the three phases. [15] - [17].

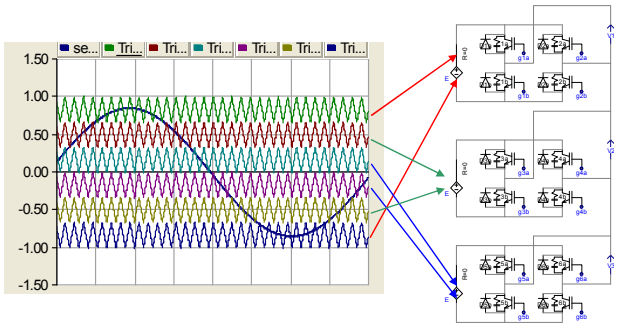


Fig. 8. Assigning of Trigger Signals According IPDPWM Modulation.

When a fault occurs, you have to isolate or stop switching the cell with fault, so if the fault occurs in the cell at the top should be left to switch the IGBTs of this cell, this can be achieved by cutting the sine wave, as shown in Fig. 9. The other phases should offset the energy delivering damaged cell, so that the reference signals for the other phases also will change. Fig.10a shows the time when the phases B and C assume the energy that gave the cell with fault. The Fig.10b shows the phase voltages and line voltage.

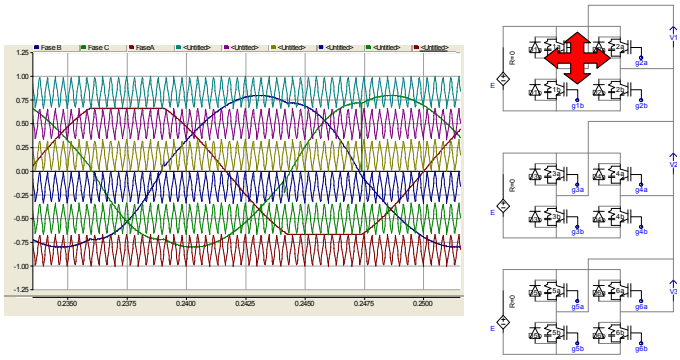


Fig. 9. Assigning of Trigger Signals – Reconfiguration

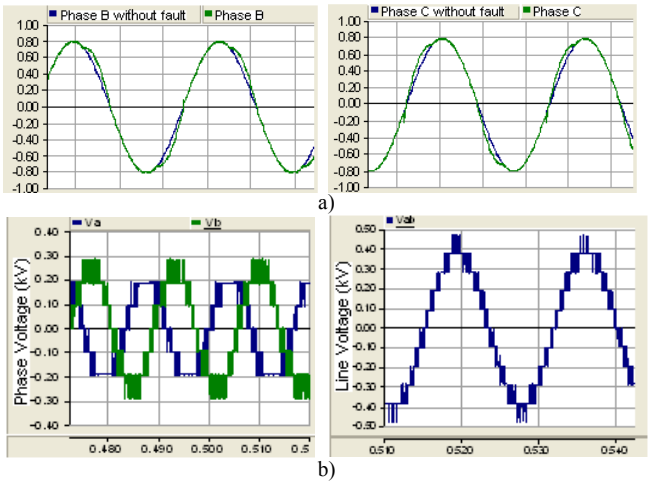


Fig. 10. Simulation results a) Phases B and C assume Energy that it is not given by the Cell in fault, b) Phase and line voltages in the engine.

The expressions for the reference signals are shown in Table II, based on [17], but with some modifications.

TABLE II
REFERENCE SIGNALS

Limite de ωt	$V_m a(\omega t)$	$V_m b(\omega t)$	$V_m c(\omega t)$
$asen\left[\frac{N-3}{M(N-1)}\right], \pi - asen\left[\frac{N-3}{M(N-1)}\right]$	$\frac{N-3}{N-1}$	$\frac{N-3}{N-1} - \sqrt{3}M.sen(\omega t + \pi/6)$	$\frac{N-3}{N-1} + \sqrt{3}Msen(\omega t + 5\pi/6)$
$\pi + asen\left[\frac{N-3}{M(N-1)}\right], 2\pi - asen\left[\frac{N-3}{M(N-1)}\right]$	$\frac{3-N}{N-1}$	$\frac{N-3}{1-N} - \sqrt{3}M.sen(\omega t + \pi/6)$	$\frac{N-3}{1-N} + \sqrt{3}Msen(\omega t + 11\pi/6)$
Otros límites	$Msen(\omega t)$	$Msen(\omega t - 2\pi/3)$	$Msen(\omega t - 4\pi/3)$

B. *Fault in two Switching Device*

Fig. 11 represents the system when two cells fail regardless of the components of each cell have failed either open circuit mode or short circuit.

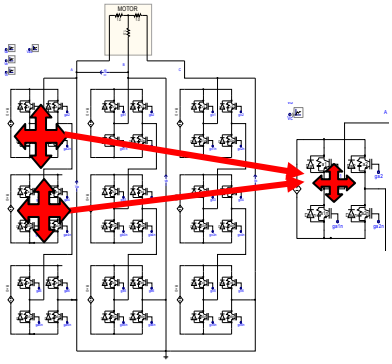


Fig. 11. Fault of two switching devices.

The expressions for the reference signals are shown in the following table, based on [17], but with some modifications.

TABLE III
REFERENCE SIGNALS

Limite de ωt	$V_m a(\omega t)$	$V_m b(\omega t)$	$V_m c(\omega t)$
$asen\left[\frac{N-5}{M(N-1)}\right], \pi - asen\left[\frac{N-5}{M(N-1)}\right]$	$\frac{N-5}{N-1}$	$\frac{N-5}{N-1} - \sqrt{3}M.sen(\omega t + \pi/6)$	$\frac{N-5}{N-1} + \sqrt{3}Msen(\omega t + 5\pi/6)$
$\pi + asen\left[\frac{N-5}{M(N-1)}\right], 2\pi - asen\left[\frac{N-5}{M(N-1)}\right]$	$\frac{5-N}{N-1}$	$\frac{N-5}{1-N} - \sqrt{3}M.sen(\omega t + \pi/6)$	$\frac{N-5}{1-N} + \sqrt{3}Msen(\omega t + 11\pi/6)$
Otros límites	$Msen(\omega t)$	$Msen(\omega t - 2\pi/3)$	$Msen(\omega t - 4\pi/3)$

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Fig. 12 shows the new reference signals and IPDPWM modulation. Fig.13a shows the time when the phases B and C assume the energy that gave the cell with fault. Fig.11c shows the phase voltages and line voltage.

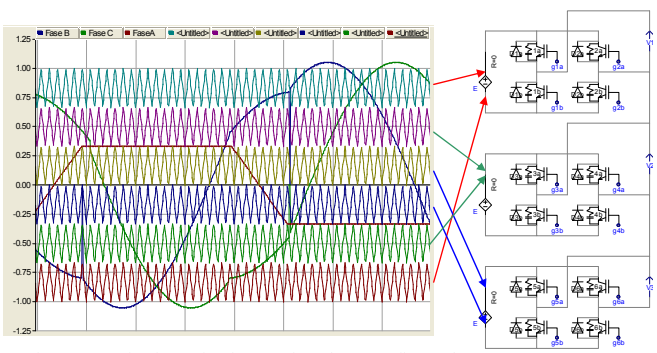

Fig. 12. Assigning of Trigger Signals reconfigured

As indicated in Table III, in a period we have five differentiated intervals in the reference signal. As we should reproduce each reference signal per phase.

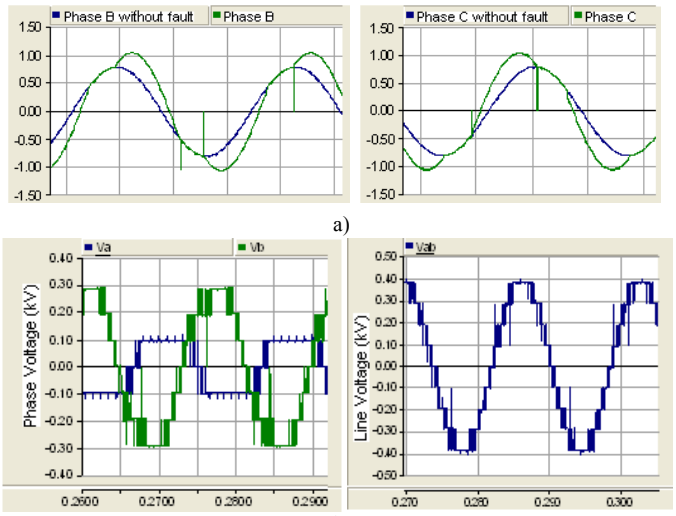

Fig. 13. Assigning of Trigger Signals: a) Phases B and C assume Energy that is not given by the cell in fault b) phase and line voltages in the engine.

VIII. IMPLEMENTATION OF STRATEGIES IN A MINING ELECTRICAL SUBSYSTEM

A. *System Description*

The electrical system where the strategy was applied belongs to a large mining company in Peru. Fig.14 shows the electrical subsystem that powers the inverter in the concentrator plant, the system consists of transformer - inverter - engine (4.16kV-1.360MVA - Engine 2.3kV) and Fig.15 shows the simulation results.

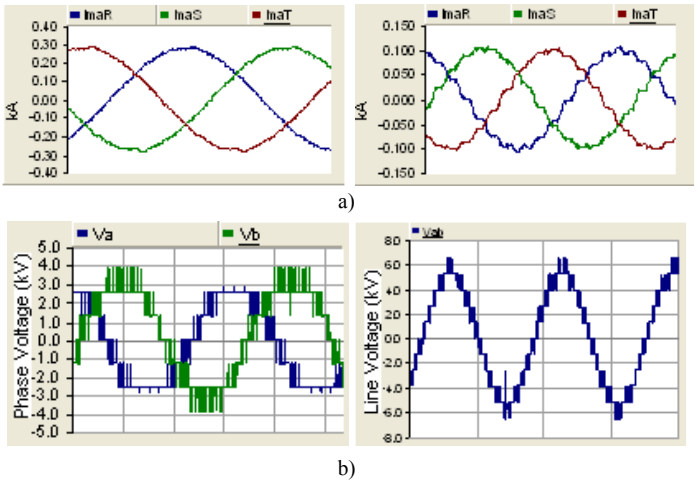

Fig. 15. Simulation results: a) Currents in Engine for before and after applying the three levels NPC strategy b) Voltages for CHB Seven Level

The inverter stage is NPC three level topology. The engine is about 1400HP, with squirrel cage double rotor and the installation height is 2800 m.a.s.l,

The simulation shows that the current in the engine is balanced. Fig. 14b shows the results of the voltage in the engine by changing the inverter stage by a multilevel inverter CHB of seven levels.

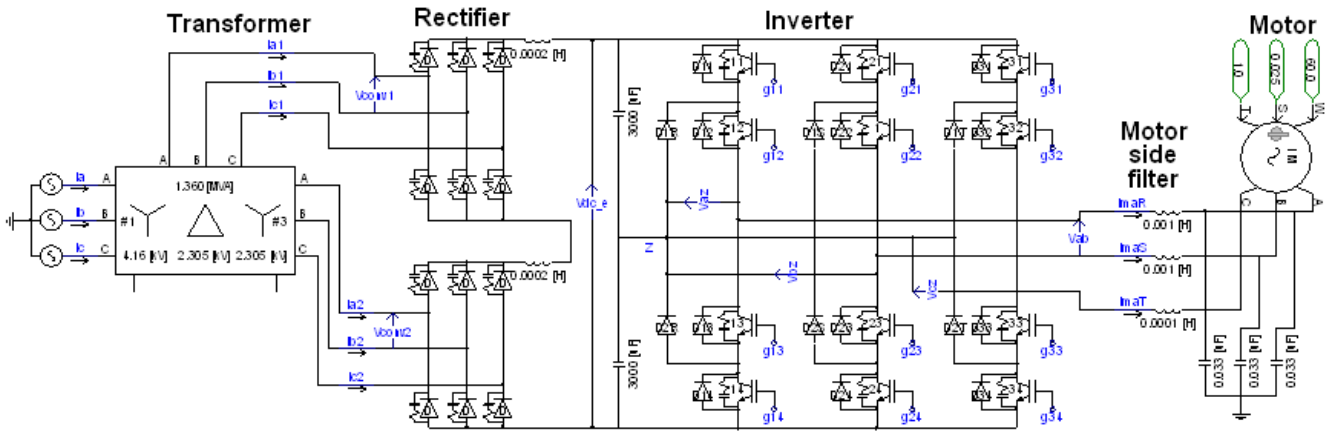

Fig. 14. System Configuration

IX. Conclusions

• The operating strategies of inverters with tolerance to faults have been studied mainly with material redundancy. However, the results obtained with the reconfiguration of the trigger signals are satisfactory especially in the strategy shown for seven-level CHB, where for the fault of a cell, the reconfiguration strategy ensures that the engine has balanced terminal voltages of same magnitude as before fault produces.

• The results obtained with the reconfiguration strategy of trigger signals for the three-level NPC inverter are satisfactory, here you get to the line voltages in the engine terminals are balanced. The voltage magnitude is less than that produced it had before the fault, but the engine can operate with less power and the production process would not stop. These operating conditions are possible as indicated by the operators of the mining electrical system taken as implementation of the strategy.

• It is important to investigate algorithms or systems that allow rapid detection of faults, as this is essential for good performance of trigger signals reconfiguration system.

X. Acknowledgements

I want to thank to MINEM - CARELEC for subsidizing my master studies and every one of the people who have supported me in the development of this work.

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