Increasing Power Capability in MOSFETs by Capacitive Coupling of Gate Signals

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***Abstract*—High voltage pulsed power supplies generate pulsed electric fields, which are widely used in biotechnology applications. Since, properties of waveform generated implied efficient. However, a current an challenging problem is limitations in the maximum operating voltage and the pulse generation with very short pulse-widths in design and implementation. Therefore, in this paper is proposed a pulsed power supply of 3 kV and adjustable pulse widths between 1 μs and 100 μs. The design is based on a MOSFET network configuration. Proposed configuration is tested and compared with a single MOSFET circuit. Finally, experimental set-up is implemented and tested through variations in load resistance and output resistance of driver MOSFET in order to verify performance of MOSFETs in proposed configuration and evaluate effects on parameters that define pulse shape as rise time, fall time, amplitude and pulse width.**

***Index Terms*—Pulsed electric field, high voltage, MOSFET, pulsed power supply, driver MOSFET, fall time, rise time.**

I. Introduction

High voltage pulsed power supplies allows generation of pulsed electric fields which are widely used for electroporation process (for further details see [1]) in biomedicine [2], [3] and biotechnology applications as in liquid food processing [4], [5]. Among the many pulse parameters, the most important that influence liquid food proccessing are: amplitude (electric field strength [6], [7]), width and shape (rectangular pulses [8]). Typically amplitudes are higher than 3 kV (to generate electric fields over 10 kV/cm [9]) with variable pulse widths regularly ranging from 1 μs to 100 μs.

Recent trends suggest to use solid-state devices since they offer many advantages, such as improved stability, high reliability, lower cost, and simpler triggering. However, Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) warrant optimus performance to high speed switching, consecuently, in this paper MOSFETs are studied. This devices show drawbacks in operating voltage (up to 1.5 kV) and current (up to 8 A). In order to take advantage of MOSFETs in high speed switching, a configuration to increase their capabilities of voltage and current is proposed.

In [10], configurations of MOSFETs in series have been proposed to increase operating voltage values; neverthless, these have limitations in operating current values. The main contribution of the paper is to overcount constraint with a configuration method of coupling MOSFETs in series and parallel. It allows voltage values up to 3 kV and pulsed currents up to 50 A: In addition, it enables increasing operating values to generalize the proposed method for n coupled MOSFETs. In this paper, complexity and number of components in circuit is minimize to use a single trigger signal and it uses a gateside technique by MOSFET's internal capacitances to achieve synchronization of gate signals.

This configuration focuses on application of pulsed electric fields allowing improving efficiency in the treatment. Being the improvement of the generated waveform, this article is directly related with power quality.

II. Description of Coupling MOSFETs Method Proposed

In [11], a coupling method MOSFETs in series to increase the operating voltage value is proposed. In this paper, the approach described is generalized for parallel and series configurations, taking into account additional design aspects. A detailed view is shown in Fig. 1, this takes into account the effects of intrinsic parasitic capacitances of the devices located in the upper part of the circuit. Effects in devices for the bottom are minimized in driver MOSFET design.

This configuration consists of parallel arrays of devices that are connected in series together. The drain of an arrangement of devices is connected to source of its neighbor, the lower array is connected to ground. A capacitor is added to common gate of each arrangement, excepting the lower arrangement, which is connected to the activation signal from driver MOSFET. Note, that a simple circuit protection for gate MOSFETs with a zenner diode is included.

A. Calculation of Coupling Capacitance

The method consists of calculating the capacitance value located at the common gate of each array. According to the details shown in Fig. 1 and taking into account Miller effect for feedback systems, voltage gain of M_{12} and M_{22} is defined as a rate between the change of drain-source voltage of M_{11}

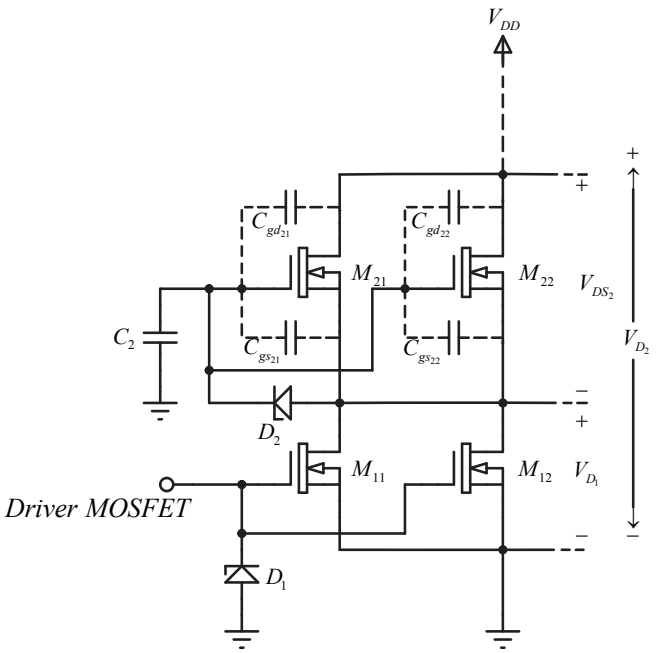

Fig. 1. Schematic of MOSFETs connection in proposed configuration.

and M_{12} (ΔV_{D_1}) and the change in gate-source voltage in M_{21} and M_{22} (ΔV_{GS_2}):

$$A_{V_2} = \frac{\Delta V_{D_1}}{\Delta V_{GS_2}} \tag{1}$$

Neglecting drain-source capacitance in MOSFETs (C_{ds21}, C_{ds22}), effective gate-source capacitance can be calculated according to:

$$C'_{gs2} = C_{gs_{21}} + C_{gs_{22}} + C_{zenner} + A_{V_2}(C_{gd_{21}} + C_{gd_{22}}) \tag{2}$$

Where, C_{zenner} is capacitance of zenner diode (D_2 in Fig. 1) placed between gate and source of the MOSFET to protect gate oxide from overvoltage. Note, that fourth term in (2) is the Miller capacitance. moreover, the change in voltage ΔV_{GS_2}, is given by:

$$\Delta V_{GS_2} = \frac{\Delta V_{D_1} C_2}{C_2 + C'_{gs2}} \tag{3}$$

Expressing C_2 from (3):

$$C_2 = \frac{\Delta V_{GS_2} C'_{gs2}}{\Delta V_{D_1} - \Delta V_{GS_2}} \tag{4}$$

C_2 allows simultaneous and synchronous switching of MOSFETs configurations with a single trigger signal. Similarly, voltage relationships for a third array of MOSFETs can be described, so A_{V_3}, is given by voltage relations ΔV_{D_2} and ΔV_{GS_3}. In circuit, if applied voltage V_{DD}, is equally divided to each arrays in series, then:

$$\Delta V_{D_2} = 2\Delta V_{D_1} \tag{5}$$

Therefore, by adding a third array, the value of coupling capacitance is:

$$C_3 = \frac{1}{2} C_2 \tag{6}$$

In general, for a series string of n parallel arrangments of MOSFETs with the same characteristics, coupling capacitance value for the $n-th$ array would be given by the equation 7:

$$C_n = \frac{1}{(n-1)} C_2 \tag{7}$$

In power MOSFETs $C_{gs} \approx C_{iss}$ and $C_{gd} \approx C_{rss}$, in MOSFET textit STW9N150, these values are 3255 pF and 22.4 pF, respectively from datasheet provided by the manufacturer. The circuit is shown in Fig. 1, in the operating voltage is 2.8 kV, so ΔV_{D_1}, is 1.4 kV. ΔV_{GS_2} value is determined by the voltage drop in the protection diode, which in this case corresponds to 18 V.

As in [12] a resistive divider that stabilizes the voltage rise at turn-off is added. Such a resistive divider is a common fixture when semiconductor devices in series are connected. MOSFETs have a positive temperature coefficient, so its parallel operation is facilitated, because if one of these leads more current, will heat up increasing its conduction resistance $R_{DS_{ON}}$ displacing current value to others devices. It also takes into account the symmetry in the construction of the experimental design (routing sizes and lengths of connecting cables same on all devices arranged in parallel) to avoid unbalances [13]. From equation 2, effective input capacitance for MOSFETs M_{21} and M_{22} in parallel (Fig. 1) has a value of 10.29 nF, finally, the value of coupling capacitance is: $C_2 = 125$ pF.

III. Design of High Voltage Pulsed Power Supply

Proposed configuration method is implemented as an essential part of a high voltage pulsed power supply and it is tested in a model application of electroporation in liquid foods. The diagram of the equipment is shown in Fig. 2

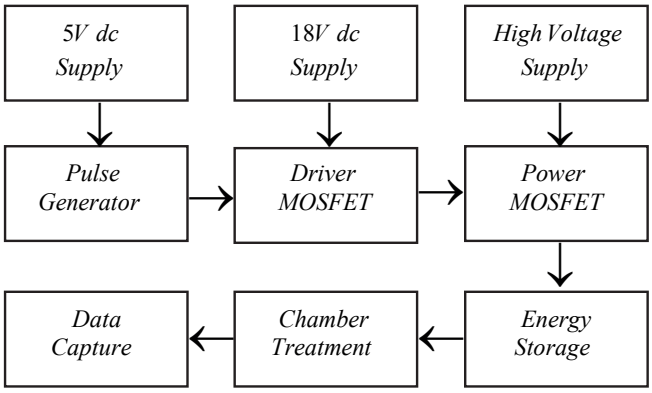

Fig. 2. Block diagram of the process.

These stages are explained below:

High voltage power supply (Fig. 2) is composed by a single-phase transformer 120 : 4000 V, input is regulated by a single-phase variable autotransformer. A diode bridge (rectification stage) and a capacitor (ripple filtering stage) is connected to output and 3 kV dc are obtained (V_{DD} in Fig. 1). 5 V y 18 V are delivered from a regulated dc power supply.

In *Pulse Generator* (Fig. 2), pulse width and number of pulses per second are programmed by firmware. In order to obtain accuracy in control of generated pulses parameters Microcontroller used is PIC18F4550. Microcontroller produces an output current value less than that required to charging MOSFET's input capacitance with speed needed.

Driver MOSFET (Fig. 2) is a power amplifier with a low-power input from microcontroller and produces a high-current drive input for MOSFET's gate, in this way, MOSFET's input capacitance can be charged quickly. Driver MOSFET *TC4424* is used.

In *Power MOSFET* (Fig. 2), proposed configuration is developed.

In *Energy storage* (Fig. 2), a capacitor is used, its capacitance value is calculated taking into account the energy requirements of the load. In this research, a capacitance value of 1μF was used.

Treatment chamber (Fig. 2) with liquid to be treated were modeled by a parallel circuit RC [14], (R_L y C_L in Fig. 3) capacitance is a constant and small value. Variations in medium conductivity can be studied by varying the load resistance (R_L).

Data capture (Fig. 2) in experimental setup was performed using an oscilloscope *TDS2014, Tektronix* and a high voltage probe *Tektronix P6015A, 1000X*.

Fig. 3 shows complete circuit of high voltage pulsed power supply.

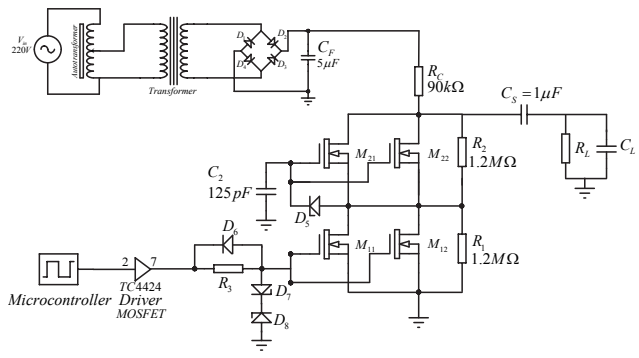

Fig. 3. Pulsed Power High Voltage Circuit.

IV. Simulation Results

Simulations were performed in order to verify the operation of proposed design. Software *PROTEUS VSM* of *Labcenter Electronics* was used. Finally, a comparison graph of switching times of proposed configuration with a single MOSFET circuit is performed.

A. Trigger Synchronization

In Figs. 4 and 5 can be seen as dividing the voltage in each of the arrays of MOSFETs connected in Fig. 3 when pass cut-off to saturation and saturation to cut-off respectively. The test is done with $R_L = 720\,\Omega$ and $C_L = 50$ pF, input voltage is 2.8 kV and capacitor C_S is 1 μF. In Figs. 4 and 5, red signal corresponds to voltage in upper MOSFETs array (M_{21}, M_{22}) and green signal corresponds to voltage in lower array (M_{11}, M_{12}).

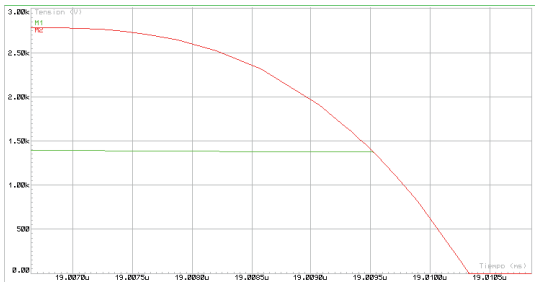

Fig. 4. Voltage drop when MOSFETs pass cut-off to saturation.

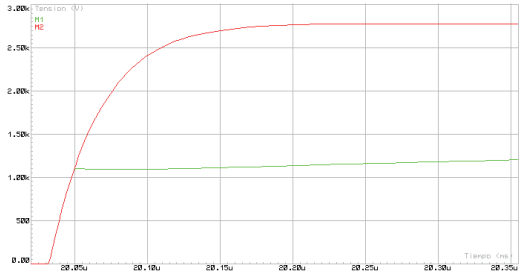

Fig. 5. Voltage drop when MOSFETs pass saturation to cut-off.

In Figs. 4 and 5 is shown that proposed configuration method ensures the same voltage level in two arrays of devices. That same rate is recorded regardless of the load resistance value.

B. Comparison of Rise and Fall Times

In this test, making variations in load resistance from 60 Ω to 720 Ω. Test conditions are the same for both circuits except for the operating voltage due to limitations of device, in this case a single MOSFET circuit operated with 1.4 kV, while power supply for proposed configuration is 2.8 kV. In Fig. 6 is shown a high voltage pulsed power supply with single MOSFET.

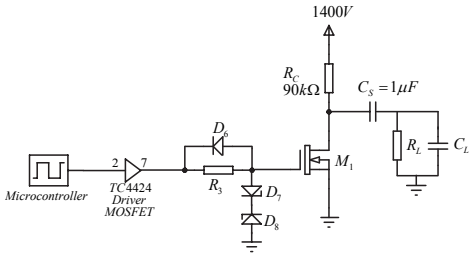

Fig. 6. High Voltage Pulsed Power Supply with Single MOSFET

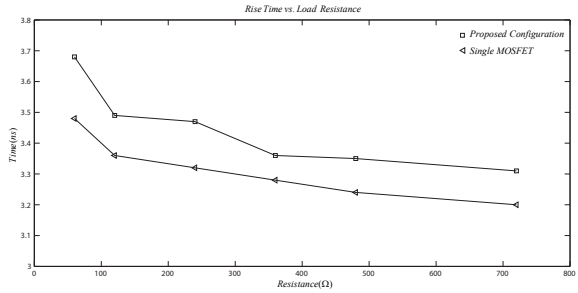

Fig. 7. Comparison of rise times

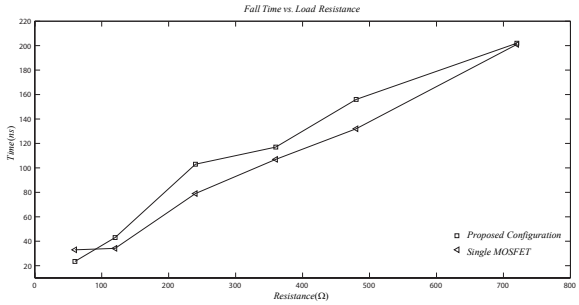

Fig. 8. Comparison of fall times

According to results shown in Fig. 7, rise times are similar for the two circuits, although, can be noticed that values obtained in the proposed configuration are slightly higher than those achieved with single MOSFET circuit. In fall times shown in Fig. 8 are observed slightly higher values for configuration proposed. Increases in the switching times are due to the input capacitance in proposed configuration is greater than in single MOSFET circuit, thus requiring a longer time for charging and discharging to be given state change in MOSFETs.

V. Experimental Results

In order to validate results obtained by simulation, tests are performed overall operation of experimental set-up, checking parameters pulses changes (rise and fall times, width, amplitude) when load resistance and output resistance in driver MOSFET change. In Fig. 9 is shown the experimental setup. Data are measured using the *Tektronix P6015A 1000X* high voltage probe and the *Tektronix TDS 2014 100 MHz* oscilloscope.

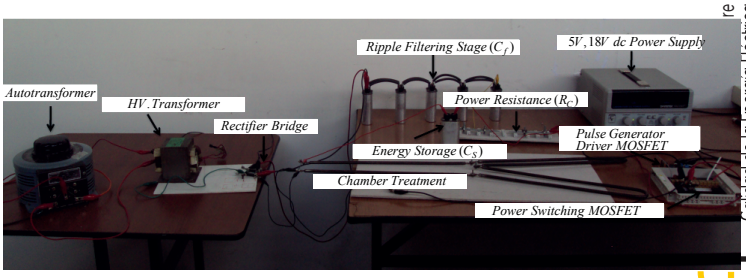

Fig. 9. Experimental set-up of High Voltage Pulsed Power Supply.

A. Comparison of Rise and Fall Times

As in the simulation section, experimental comparison is done at the time of rise and fall. Output waveform for a pulsed power supply with single MOSFET is shown in Fig. 10 and comparison results are shown in Figs 11 and 12.

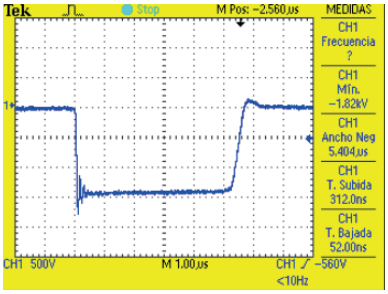

Fig. 10. Output waveform High Voltage Pulsed Power Supply with Single MOSFET

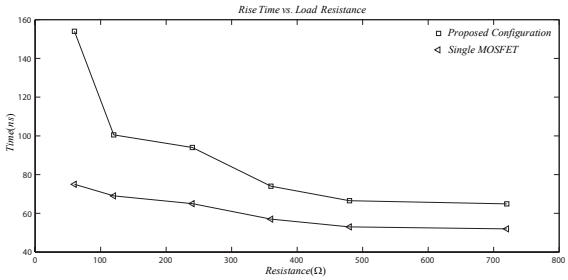

Fig. 11. Comparison of rise times

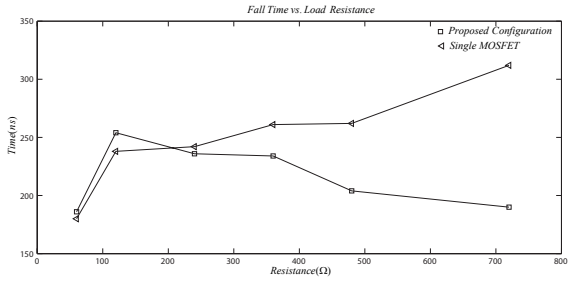

Fig. 12. Comparison of fall times

B. Variations in Load Resistance

Conductivity is one feature to consider in liquid foods for pulsed electric field process. This value is inversely propor-

tional to the load resistance. When performing this variation aims to evaluate the dependence of output pulse shape on the conductivity of the medium being treated. The value of load capacitance is constant and depends on the construction characteristics of the treatment chamber, in this research uses a value of 50 pF. In Figs. 13 and 14 are observed waveforms obtained for values of $R_L = 720\,\Omega$ and $R_L = 120\,\Omega$, respectively.

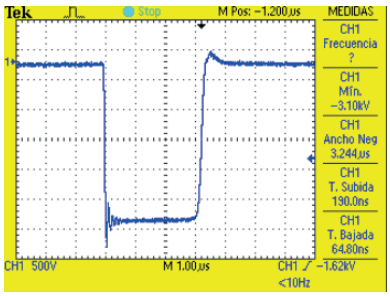

Fig. 13. Output waveform High Voltage Pulsed Power Supply for $R_L = 720\,\Omega$.

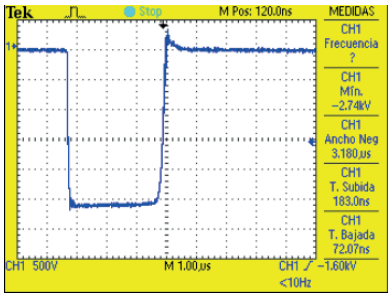

Fig. 14. Output waveform High Voltage Pulsed Power Supply for $R_L = 120\,\Omega$.

In Figs. 15, 16, 17 and 18 shows effects of variation of resistance on amplitude, rise time, fall time and pulse width respectively.

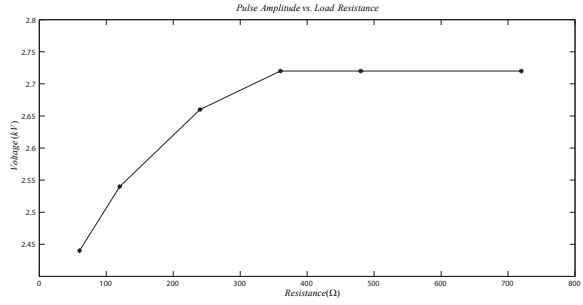

Fig. 15. Effect of load resistance variation (R_L) on pulse amplitude.

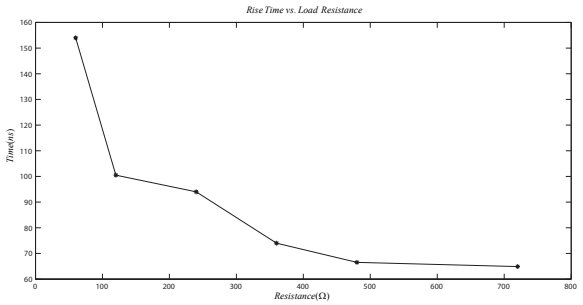

Fig. 16. Effect of load resistance variation (R_L) on rise times

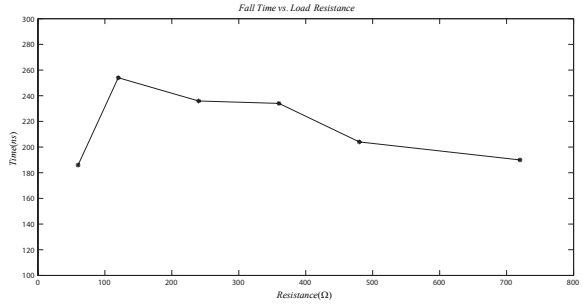

Fig. 17. Effect of load resistance variation (R_L) on fall times

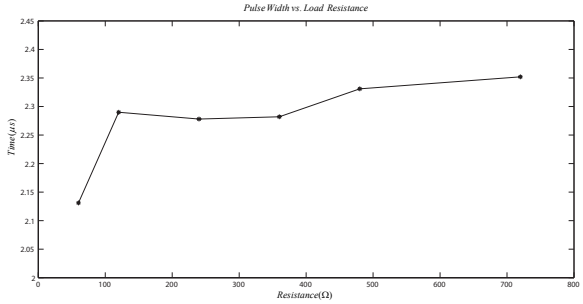

Fig. 18. Effect of load resistance variation (R_L) on pulse width.

For Fig. 15 decrements in amplitude for low values in load resistance are observed. These are due to the fact that the lower resistance value more energy will require in energy storage capacitor C_S to keep a constant voltage value for duration of the pulse. Moreover, in the smaller load resistance will approximate the equivalent resistance of MOSFETs in conduction. The resistance in conduction mode of the proposed configuration is equivalent to the resistance of a single MOSFET (1.8 Ω for STW9N150), so the amplitude is not affected significantly and conduction losses reduces.

For rise times, the experimental results do not make a direct increase. The most notable changes occur in fall times and these show that lower resistance value lower that time. Difference between maximum and minimum fall time was 68 ns, while for the rise time was 89 ns.

C. Variations of Output Resistance in Driver MOSFET

In this section effects on pulse parameters when values of output resistance in driver MOSFET change are observed. The range of variation was selected taking into account limitations of MOSFETs, because if the rise and fall times are too long, the device will experience overheating causing their destruction. The range of variation is given between $1\,\Omega$ and $47\,\Omega$. In Figs. 19 and 20 waveforms by a resistance value output of $1\,\Omega$ and $47\,\Omega$, respectively, with a load resistance $R_L = 720\,\Omega$ are observed.

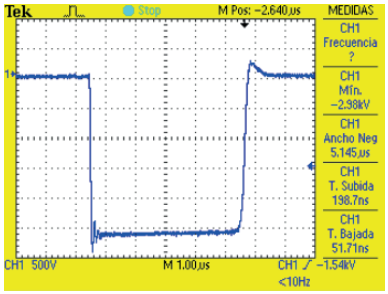

Fig. 19. Output waveform High Voltage Pulsed Power Supply for $R_3 = 1\,\Omega$.

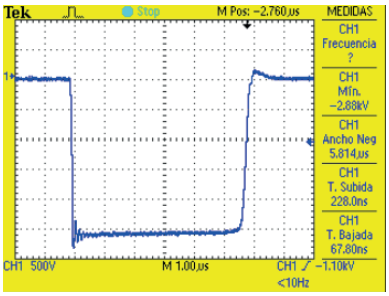

Fig. 20. Output waveform High Voltage Pulsed Power Supplyfor $R_3 = 47\,\Omega$.

In Figs. 21, 22, 23 and 24 shows effects of variation of resistance on amplitude, rise time, fall time and pulse width respectively.

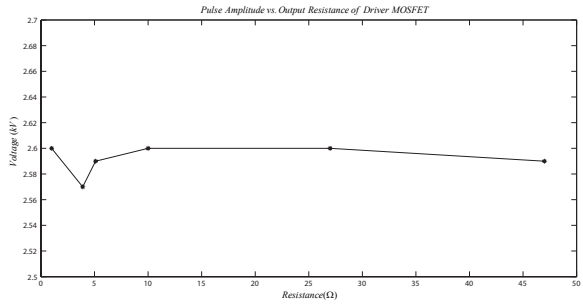

Fig. 21. Effect of output resistance in Driver MOSFET variation (R_3) on pulse amplitude.

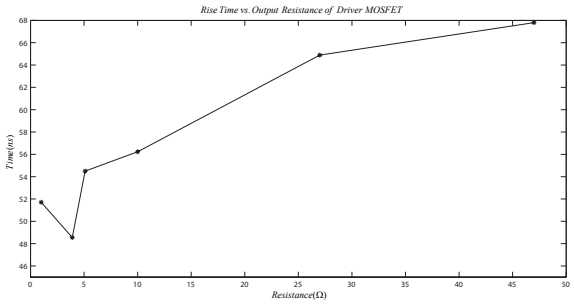

Fig. 22. Effect of output resistance in Driver MOSFET variation (R_3) on rise times

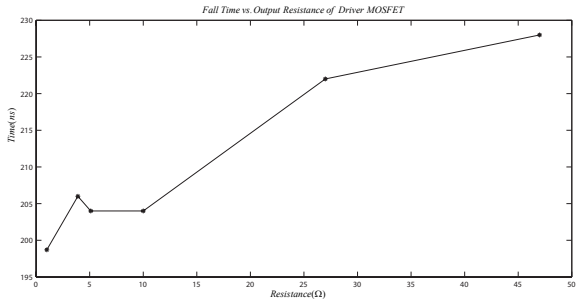

Fig. 23. Effect of output resistance in Driver MOSFET variation (R_3) on fall times

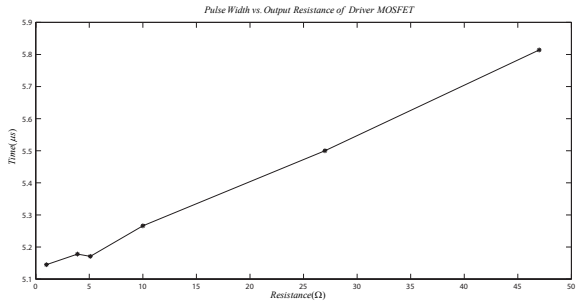

Fig. 24. Effect of output resistance in Driver MOSFET variation (R_3) on pulse width.

According to Figs. 22 and 23, there is a linear relation between increase in output resistance in driver MOSFET and increase in rise and fall times. Pulse amplitude is not affected by the variation in such resistance. In Fig. 24 can be demonstrated that the pulse width is changed significantly with variation. Variations reach 669 ns in the entire range, value much higher than those achieved when making variations in load resistance. Same test with variations in parameters were done in simulations, similar to comparing rise an fall times with pulsed power supply with single MOSFET, difference between simulated and experimental data were found. The difference are probably due to the limitations of the MOSFET model used in *Proteus VSM*, however, the trend matches. Increase in rise and fall times shows importance of output current of driver MOSFET in pulse shape for aplication and

reducing switching losses. These tests also were conducted through simulation, further changes were made in capacitance of energy storage circuit. To perform this variation was found that the lower the capacitance value was smaller the amplitude.

VI. Discussion and Conclusions

We have proposed a novel technique for increasing the power capability, increasing operating voltage and current taking advantage in switching features of devices, using MOSFET technology. The numerical results were validated with experimental set-up.

A comparison between two configurations (Single MOSFET and Configuration Proposed), reveals a slightly difference. For example in rise-time intervals, the maximal difference is aproximatelly 28.3%, while in fall-time a maximum difference of 6.7% is recorded. Increases are due to driver MOSFET for proposed configuration must control two parallel MOSFETs, and more current is required.

As lower the resistance value will require more energy in the capacitor C_S to keep the voltage constant during the pulse time. Moreover, in small load resistance, its value is similar to equivalent resistance of MOSFETs in conduction mode. As a result, voltage reduction will be more significant at low resistance values. In configuration proposed the equivalent resistance is equal to a single MOSFET, ($1.8\,\Omega$), and reduction achieved for minimum resistance value is approximately 12% and condution losses is minimal. With specifications of the treatment chamber it is possible to generate electric fields on limits defined for use in liquid foods (10 kV/cm and 80kV/cm [9]).

We have found that output resistance of driver MOSFET (R_3) plays a key role in the waveform. That stabilize transient oscillations in the MOSFET ON-OFF state (MOSFET gate protection against overvoltage), but this increase rise and fall times of the pulse. Therefore, a suitable value of this resistor must be considered. Under this restriction, the resistance value used in this paper was $3.9\,\Omega$. Experimental results provides the possibility of using a driver MOSFET which handles higher current values (> 3 A) to improve rise and fall times and reduce switching losses.

Transient oscillations in the MOSFET ON-OFF state has been observed. This may be caused by parasitic inductances formed by interconnection of elements in series, distances between connecting points (wire lengths) and inductive characteristics of some resistors used in the source. Consecuently, these oscillations may extent rise and fall times.

Acknowledgment

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