Performance of True-48-Pulse DSTATCOM for Voltage Sag Mitigation

Desempeño de un DSTATCOM de 48-pulsos para la mitigación de hundimientos de tensión

O. F. Orjuela[1], H. E. Rojas[2], D. A. Gutierrez[3]

ABSTRACT

This paper presents the implementation and performance of three-phase Distribution Static Compensator (DSTATCOM) used for voltage sag mitigation. The DSTATCOM is based on a voltage source SPWM inverter with a true-48-pulse circuit-level. For simulations, IEEE-34 bus test feeder is chosen due to its topological features and wide variety of components. Simulations using ATP/EMTP software describe the DSTATCOM design process and provide experimental results. In addition, the performance of DSTATCOM in several cases is analyzed, showing that this device is a good alternative for power quality improvement in distribution systems.

Keywords: 48-pulse inverter, ATP/EMTP, DSTATCOM, IEEE-34 bus-test-feeder, sags mitigation, SPWM modulation

RESUMEN

Este artículo presenta la implementación y desempeño de un compensador estático de distribución trifásico (DSTATCOM) usado para la mitigación de hundimientos de tensión (sags). El DSTATCOM se basa en un inversor trifásico con modulacion por ancho de pulso senoidal (SPWM) con un circuito multinivel de 48 pulsos. Para las simulaciones se seleccionó el sistema de distribución IEEE-34 debido a sus características topológicas y una amplia variedad de componentes. Simulaciones usando el software ATP/EMTP describen el proceso de diselo del DSTATCOM y proporcionan resultados experimentales. Adicionalmente, el desempeño del DSTATCOM es analizado en varios casos mostrando que este dispositivo es una buena alternativa para mejorar la calidad de potencia en sistemas de distribución.

Palabras clave: ATP/EMTP, DSTATCOM, inversor de 48 pulsos, mitigación de sags, modulación SPWM, sistema IEEE-34

Received: July 22th, 2015
Accepted: Sept 24th, 2015

Introduction

A power distribution network can be affected by current and voltage-related power quality (PQ) problems such as distorted current sources and voltage disturbances (Bollen, 1999). Voltage sag is a short-duration reduction in RMS voltage between 10% and 90% of the nominal value with duration from half-cycle to a few seconds. These disturbance produce mal-operation or interruption on sensitive equipment, many times leads to complete interruptions of the industrial process and affect the proper operation of power and distribution systems.

[1] Oscar Felipe Orjuela-Sastoque. Electrical Engineering Student, Universidad Distrital Francisco José de Caldas, Colombia. Electromagnetic Compatibility and Interference Group GCEM, Colombia. E-mail: oscaror-9@hotmail.com

[2] Herbert Enrique Rojas-Cubides. Electrical Engineer, M.Sc. in Electrical Engineering and candidate to Ph.D. from Universidad Nacional de Colombia, Colombia. Assistant Professor in Electrical Engineering Department, Universidad Distrital Francisco José de Caldas Colombia. Electromagnetic Compatibility and Interference Group GCEM. E-mail: herojasc@udistrital.edu.co

[3] David Alberto Gutierrez-Casas. Electrical Engineering Student, Universidad Distrital Francisco José de Caldas, Colombia. Electromagnetic Compatibility and Interference Group GCEM, Colombia. E-mail: ozzy_loureiro@hotmail.com

Voltage sags are caused by faults and short-circuit generally associated to bad weather conditions (i.e. lightning strokes, storms, wind, etc.), energizing of larger loads and transformers, motor starting, overloads and other load variations (Bollen, 1999). Although voltage sags are less harmful than interruptions, they are more frequent, besides their effects on sensitive devices and equipment can be as important as those produced by an interruption. For these reasons, voltage sags are among the most frequent and one of the main PQ problems (McGranaghan, Mueller, & Samotyj, 1991).

The distribution static compensator (DSTATCOM) is a shunt-connected device used to mitigate PQ problems and can operate in voltage-control mode (VCM) or in current-control mode (CCM) (Kumar & Mishra, 2014). Additionally, DSTATCOM has the capability to sustain reactive current at low voltage, reduced land use and can be developed as a voltage and frequency support by replacing capacitors with batteries as energy storage (Masdi, Mariun, Mahmud, Mohamed, & Yusuf, 2004).

This paper presents the design process and implementation of a true-48-pulse DSTATCOM for voltage sag mitigation. The suitability of DSTATCOM (operation and control scheme) is verified by simulation using Alternative Transient Program (ATP/EMTP). In order to understand the DSTATCOM performance, several case studies are presented using the IEEE-34 bus test feeder. In

addition, analysis between reactive power injected by DSTATCOM and voltage sag depth is considered.

The rest of this paper is organized as follows. The configuration, operation and modeling of DSTATCOM using ATP/EMTP are summarized in Section 2 and Section 3, respectively. Section 4 describes the DSTATCOM control methodology. In section 5, the features of IEEE-34 bus test feeder and the case studies are presented. In section 6, simulations and analysis of DSTATCOM impact on test system, under voltage sag conditions, is performed. Finally, some conclusions are presented in section 7.

Configuration and Operation of DSTATCOM

Basic structure of DSTATCOM

Static compensator DSTATCOM is a three-phase electronic power device. It is connected in shunt at distribution systems near to the load (Masdi et al., 2004). The basic structure of DSTATCOM consists of a DC energy storage device (DC source or DC capacitor), a three-phase inverter module (based on IGBT, thyristor, etc.), a control stage, an AC filter, and a step-up coupling transformer (Rojas, Cruz, & Rojas, 2015). Figure 1 shows the block diagram of DSTATCOM and its connection scheme.

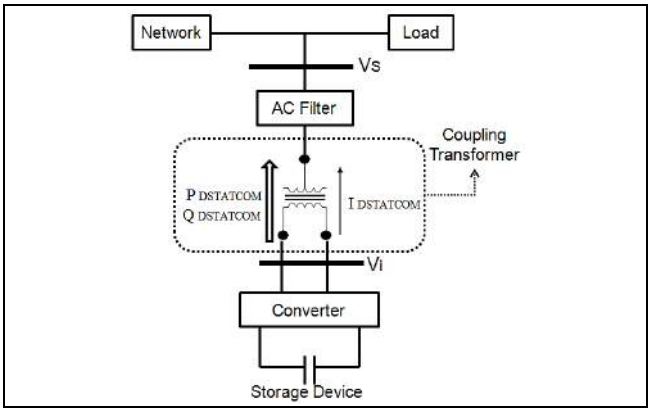


Figure 1. Block diagram of DSTATCOM
Source: Authors

Operation of the DSTATCOM

The DSTATCOM is a solid-state device with the ability to control the voltage magnitude and the phase angle, for this reason can be treated as a voltage controlled source but can also be seen as a controlled current source. The controller regulates the reactive current that flows between the compensator and the distribution system in such a way that the phase angle between the inverter voltage (Vi) and the system voltage (Vs) is dynamically adjusted so that the DSTATCOM absorbs or generates the desire reactive power at a specific point common coupling (PCC). The active power (P_{DST}) and reactive power (Q_{DST}) that flow through an impedance can be calculated using the following equations:

$$P_{DST} = [(|Vs||Vi|)/X_{Trx}] * sen(\delta) \quad (1)$$

$$Q_{DST} = [\{(|Vs||Vi|)/X_{Trx}\} * cos(\delta)] - [|Vs|^2/X_{Trx}] \quad (2)$$

where, Vi is the output voltage of the DSTATCOM, Vs is the power system voltage, X_{Trx} is the reactance of the coupling transformer and δ is the phase angle between Vi and Vs. Equations (1) and (2) show that the basic operation of DSTATCOM varies depending upon Vi.

DSTATCOM modelling and simulation

DC energy storage device

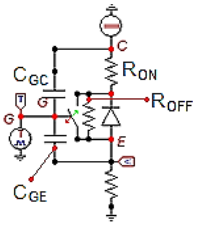
DC voltage storage device is modeling as DC source connected in parallel with a capacitor C_{DC}. The sizing of this capacitor is referred to the fault current in the system, which is defined as the different between the current before and after the fault (Masdi & Mariun, 2009). To determine the size of C_{DC} in a three-phase system the following equation is used (Hsu & Wu, 1996).

$$C_{DC} = 3 \cdot [(V_{DSTAT} * \Delta I_L * T)/(V_{C\,máx}{}^2 - V_{DC}^2)] \quad (3)$$

where, V_{DC} is the voltage across C_{DC} per phase, V_{DSTAT} is the peak voltage per phase, ΔI_L is the difference between the current before and after in the load, T is the period of one cycle of voltage and current and $V_{C\,máx}$ is the upper limit of the energy storage in C_{DC} per phase. For voltage sag conditions, the value of ΔI_L can be determine by measuring the load current before and during the disturbance (Hsu & Wu, 1996). The value of V_{DC} is determined from ATP/EMTP simulation for each case study. The value of $V_{C\,máx}$ is the upper limit of C_{DC} voltage and this can be two or three times of V_{DC}.

Power electronic stage

Usually, the DSTATCOM configuration consists of a conventional six-pulse or twelve-pulse inverter arrangement (Rojas et al., 2015). Configurations that are more sophisticated use multi-pulse or multi-level configurations. In this paper, a true-48-pulse inverter configuration is used. This configuration uses eight 6-pulse inverters connected in parallel with the same DC-source. For each six-pulse inverter, six bidirectional semiconductors are used. Figure 2 shows the configuration in ATP/EMTP for one branch that conform a six-pulse inverter.



Parameters IGBT model	
R_{ON}	0,0057 Ω
R_{OFF}	240000 Ω
C_{GC}	5,49 nF
C_{GE}	9,31 nF

Figure 2. Configuration and values of a six-pulse inverter branch
Source: Authors

For the DSTATCOM model proposed in this paper, Insulated Gate Bipolar Transistors (IGBT) are used. Followed to this element is connected a resistance in series (R_{ON}) that represents the inverter losses when the IGBT is turned-on and a resistance connected in parallel (R_{OFF}) that represents the losses when the valve is turned-off. It is important to emphasize that the inverter model includes a gate-collector capacitor (C_{GC}) and a gate-emissor capacitor (C_{GE}) that represent the parasite capacitances. Finally, to complete the IGBT basic model an ideal type-13 switch controlled by TACS is used as commutation element.

In general terms, the DSTATCOM voltage source is controlled with hysteresis or ramp comparison type current regulated PWM inverter (Muni, Rao, & Vithal, 2006). The Sinusoidal Pulse Width Modulation (SPWM) technique is widely employed in order to adjust the inverter output voltage (amplitude) and the

frequency to the desired value. In this technique, the power converter switches (implemented with IGBTs) are set to the ON or OFF state according to the result of the comparison between a high-frequency constant-amplitude triangular wave (carrier) with a low-frequency (e.g., 60 Hz) reference sine wave of adjustable amplitude and/or frequency (Lakka, Koutroulis, & Dollas, 2014).

In this study, an SPWM modulation scheme is developed. For the construction of this circuit a triangular wave generator, a sine wave signal and a comparator is required. Due to ATP/EMTP does not provide a model of triangular wave generator, a triangular signal is constructed integrating a square wave. The SPWM modulation circuit in ATPDraw is presented in Figure 3. The SPWM provides an output signal with a switching frequency of 8 KHz. In addition, Figure 4 presents a six-pulse unit inverter using in the DSTATCOM model.

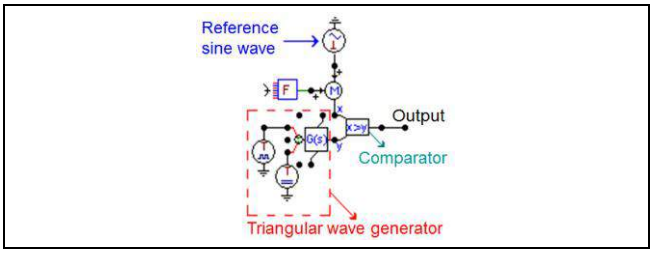


Figure 3. SPWM modulation circuit in ATPDraw
Source: Authors

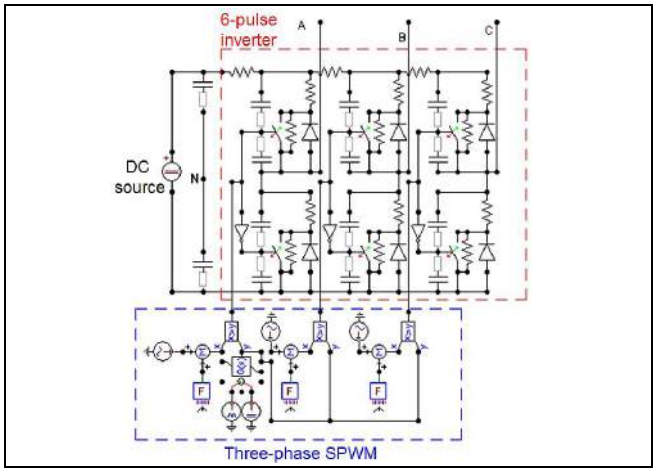


Figure 4. Six-pulse three phase unit inverter
Source: Authors

The true-48-pulses circuit for the DSTATCOM inverter uses eight intermediate transformers with a Y-Δ connection. Each 6-pulse unit has a transformer delayed 7.5° with respect to the next 6-pulse stage. The wye-connected windings of these transformers are connected in series and the windings connected in delta remove the third-harmonic components from the inverter output voltages. Figure 5 shows the connection scheme of the true-48-pulse inverter.

Figure 6 shows the line-to-line output voltage of the true-48-pulses inverter when the output of DC energy storage device is adjust to $V_{DC} = 722\,V$. In this case, the peak value of single-phase output voltage signal is 2983 V, while line-to-line output voltages reach maximum values of 5779 V. With respect to the amplitude of DC voltage, the single-phase and the line-to-line output voltages present an increase of four and eight times, respectively. In this case, the SPMW variables were placed in 1 for the amplitude modulation with a switching frequency of 8 KHz.

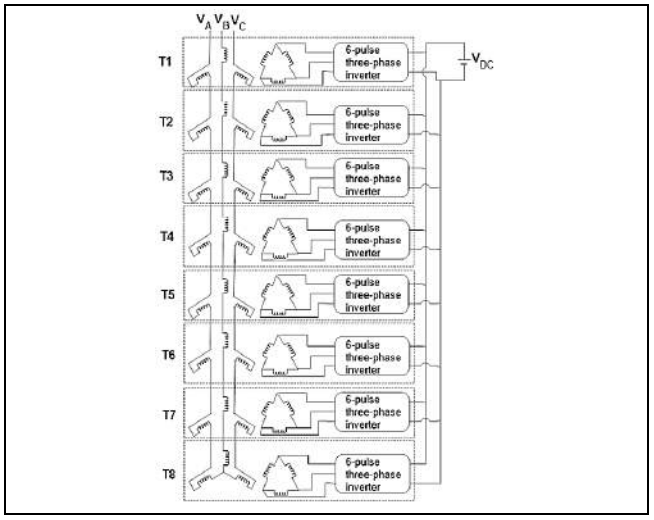


Figure 5. True-48-pulse inverter scheme
Source: Authors

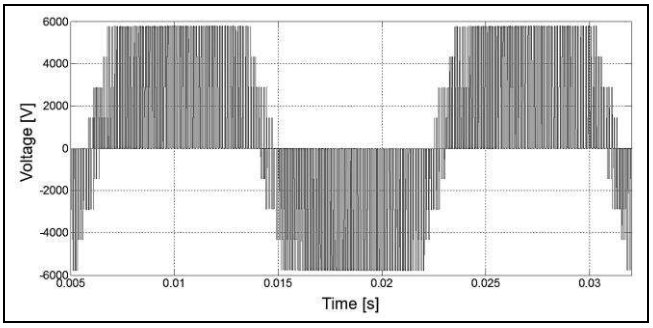


Figure 6. Line-to-line output voltage of true-48-pulse inverter
Source: Authors

The harmonic components of the single-phase output voltage of the DSTATCOM are shown in Figure 7. The analysis shows that single-phase output voltages have harmonic components between 110th and 170th order (i.e. between 6 kHz and 11 kHz). The maximum harmonic is founded in 7.98 KHz with a value of 1465 V. This output voltage presents a THDv of 80.2%.

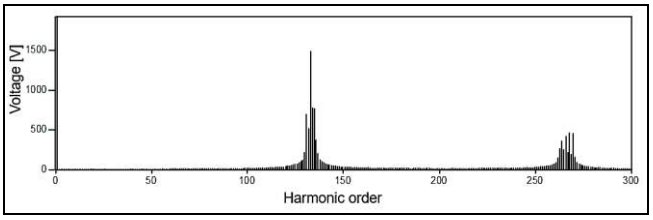


Figure 7. Harmonic components of single-phase output voltage of the true-48-pulse inverter
Source: Authors

Harmonic filter connection

Due to true-48-pulse DSTATCOM output voltages are signals composed by high-frequency harmonics, a LC low-pass filter to reduce the harmonic distortion was implemented. The values of the inductance and the capacitance of filter are 1 mH and 51 μF, respectively. The cut-off frequency of LC filter was 700 Hz and its Bode diagram is shown in Figure 8. The THDv of the filtered

output voltages is 1.24%. The peak value of single-phase output voltage is 3587 V. An example of the filtered output voltage for true-48-pulse inverter is illustrated in Figure 9.

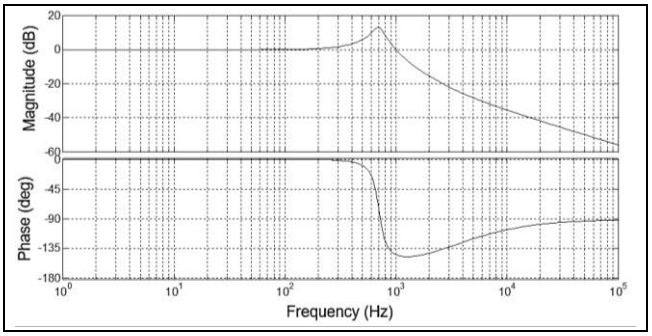


Figure 8. Bode diagram for the LC filter
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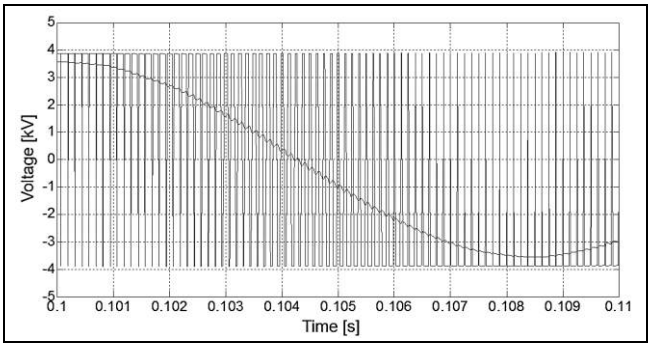

Figure 9. Single-phase output voltage of the true-48-pulse inverter. Inverter output signal (square wave), filtered signal (sine wave).
Source: Authors

Coupling transformer configuration

This device is a Y-Y transformer that allows the energy exchange between the AC system and DSTATCOM. In applications that include electronic devices the coupling transformer is used to adapt the circuit impedances, change the values of inverter output voltages and connect to the next stage. The technical features of coupling transformer are defined in section 5.

DSTATCOM control structure

The controller of DSTATCOM monitors the system behavior and governs the magnitude and phase of the output voltage signals of the inverter. The designed control scheme of DSTATCOM for voltage sag mitigation is shown in Figure 10. The phase synchronization block is composed for three single-phase PLL, which provide the synchronization angles of the DSTATCOM output signals. The reference values for the amplitude modulation process are obtained from the amplitude control. The sine wave generator takes the reference values to produce the modulation signals that feed the SPWM module.

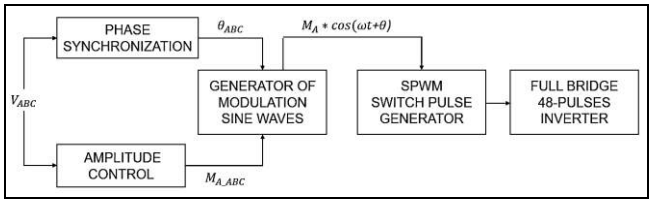

Figure 10. Block diagram of the control scheme for sag mitigation
Source: Authors

Figure 11 shows the complete circuit of the DSTATCOM for voltage sag mitigation in ATPDraw. This circuit includes the single-phase PLLs and two RMS-value meters that measure the voltages and currents of the distribution system to obtain the input signals of the model control scheme. Also, it is observed the electronic power stage (described in section 3), the LC filter and the coupling transformer.

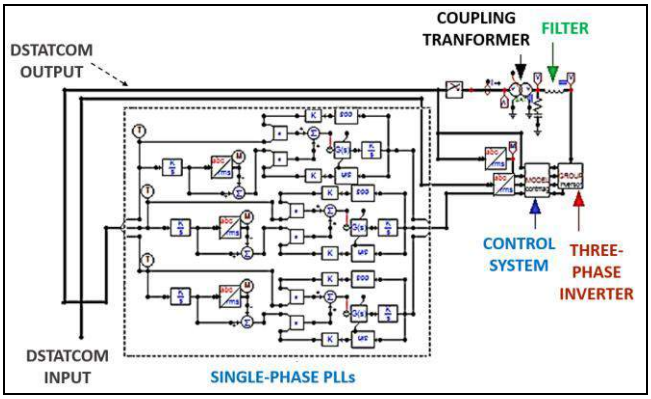

Figure 11. Control circuit for voltage sag mitigation in ATPDraw
Source: Authors

Distribution test system and case studies

IEEE-34 bus test feeder

The distribution system used in this study is based on the IEEE-34 bus test feeder. This system is chosen because of its topological features and wide variety of components. This distribution network has two voltage regulators, two capacitor banks and one low voltage lateral at 4.16 kV. The substation is rated at 2500 kVA, with a 69kV/24.9 kV transformer. Loads are modelled as three-phase (balanced or unbalanced), single-phase spot or distributed loads (IEEE Distribution System Analysis Subcommittee, 2000).

Due to IEEE-34 system is a distribution network with a radial configuration, any fault produced near to the substation transformer (node 800) significantly affects all voltage profiles of the system. To avoid this condition, the IEEE-34 system was modified connecting other substation unit, with the same characteristics of the original one, at node 846 where no loads are connected. Figure 12 shows the scheme of IEEE-34 modified system (IEEE-34M). The use of the new distributed generation (GD) unit guarantees that critical nodes are located in different points of the system reducing the relevance of nodes 800 to 814.

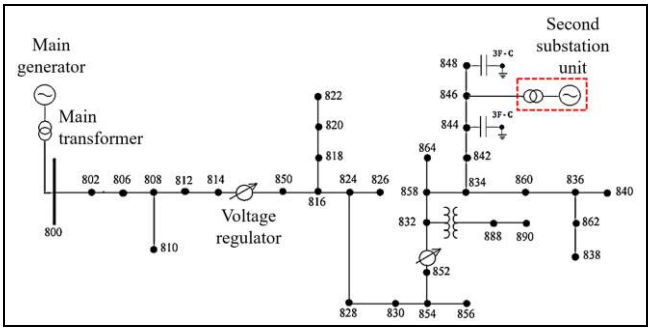

Figure 12. Scheme of IEEE-34M distribution system
Source: Authors

Case studies under PQ problems

The voltage sag conditions used in this paper were chosen using a method of stochastic generation of disturbances and assuming that voltage sags were originated only by faults. The application of this method requires the generation of random values with a probability density that are used to obtain the location of disturbance, the type of fault and the fault resistance. Applying this stochastic method, the test system has been simulated in 760 voltage sag scenarios.

The characteristics of the faults have been randomly generated with a MATLAB ® routine. In each simulation scenario, the results of fault configurations were used to estimate a local function LF. This function allows to analyze how much IEEE-34M system is affected by the occurrence of a fault condition A in a specific node k. The local function is given by:

$$LF_{Ak} = \sum_{i=1}^{13}\sum_{j=1}^{3}(V_{Ref-ij} - V_{Fault-ij})^2 \qquad (5)$$

Where, i is each node in the system, j is the phase (A, B or C), V_{Ref-ij} is the pre-fault voltage in p.u. and $V_{Fault-ij}$ is the voltage in p.u. during the voltage sag condition. Table I presents the worst cases under balanced and unbalanced voltage sags.

Table 1. Case studies for DSTATCOM implementation

Case	Node	Fault Type	Resistance Value [Ω]	Local Function	Voltage sag deep [p.u.]
1	N834	3L – 10	4	40.848	0.155
2	N842	2LG – 7	4	28.489	0.1514

Source: Authors

These are the case studies where DSTATCOM will be evaluated for voltage sags mitigation. Taking into account that the presence of voltage sags has a random nature and the most critical conditions are produced by three-line faults, the case study 1 is a valid example of the IEEE-34M system response.

Voltage sags mitigation using DSTATCOM

To analyze the response of the IEEE-34M system for each case study and to evaluate the performance of the DSTATCOM under voltage sag conditions, the following methodology is applied:

- The DSTATCOM is connected at node in which the voltage sag occurs (node with the deeper voltage)
- Evaluate the DSTATCOM response
- Analyze the DSTATCOM output voltage signals and the operation of the control scheme
- Calculate the reactive power injected by the DSTATCOM that improves the voltage profile of the IEEE-34M system and mitigates the voltage sag condition.

According to the voltage levels of the IEEE-34M system, the technical features of the coupling transformer connected to the DSTATCOM are: voltage 24.9kV/4.16kV, power 2.5 MVA, connection Y-Y and impedance 5.86%.

Case Study 1: voltage sag at node 834

In this case, a three-line fault (type 10) at node 834 with a fault resistance of 4Ω was analyzed. This scenario is the most critical of the simulated cases, producing an average voltage sag per phase of 0.155 in p.u. This voltage sag condition begins at 52.5 ms and ends at 350 ms. Figure 13, Figure 14 and Figure 15 show the voltage profile at each phase of node 834 before voltage sag (dashed line), during sag without DSTATCOM (grey line) and during sag condition with DSTATCOM (black line). It is possible to observe that DSTATCOM takes an average time of 45 ms before to starting the reactive injection.

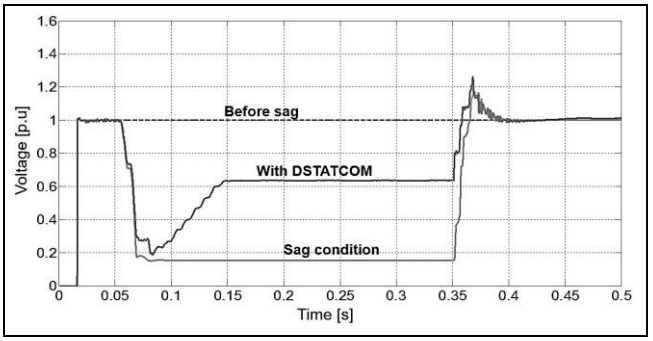

Figure 13. RMS Voltage of phase–A for case 1 (sag at node 834)
Source: Authors

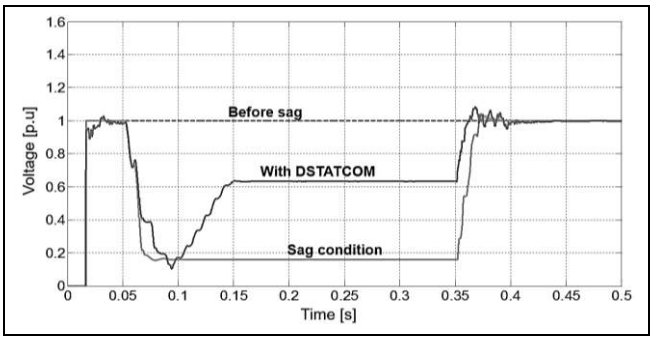

Figure 14. RMS Voltage of phase–B for case 1 (sag at node 834)
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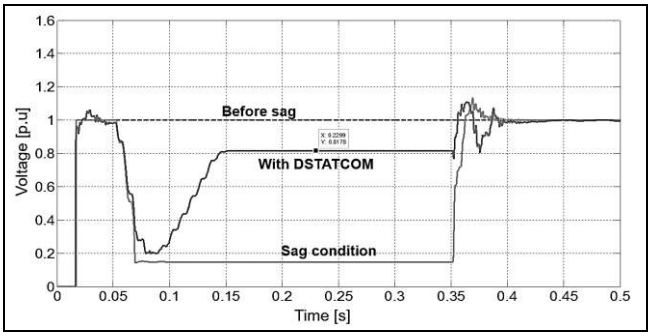

Figure 15. RMS Voltage of phase–C for case 1 (sag at node 834)
Source: Authors

In this case, the local function was reduced from 40.85 to 11.71 applying a DC voltage of 3.6 kV. In addition, the compensator improves the voltage of the node 834 reaching an average value of 0.714 p.u. per phase. With these changes, all voltages of IEEE-34M system are also improved achieving a minimum value of 0.63 p.u. at node 834 and a maximum value of 0.88 p.u. at node 890. Table 2 presents the RMS voltages per phase at the node 834 before and after the connection of DSTATCOM during the voltage sag.

Table 2. Voltage comparison at node 834 for case 1

DSTATCOM Condition	Phase A [p.u]	Phase B [p.u]	Phase C [p.u]
Without DSTATCOM	0.153	0.160	0.149
With DSTATCOM	0.664	0.631	0.817

Source: Authors

Finally, the C_{DC} value using the Eq. 3 is 148.3 μF. Finally, the reactive power of the DSTATCOM is calculated as follows:

$$Q = \omega * C_{DC} * V_{L-L}^2 \quad (4)$$

Where, $\omega = 377\ [\mathrm{rad/s}]$ and V_{L-L} is the nominal line-to-line voltage of the system at the PCC. For IEEE-34M system $V_{L-L} = 24.9\ kV$. Using the Eq. 4 the rating reactive power injected by DSTATCOM is 3462 kVAR.

Case Study 2: voltage sag at node 842

The voltage sag occurred at node 842 is due to a double-line-to-ground fault (type 7) with a resistance of 4Ω. This condition produces an average voltage sag per phase of 0.151 p.u. This voltage sag condition begins at 41.5 ms and ends at 350 ms. Figure 16, Figure 17 and Figure 18 show the voltage per phase of node 834 before voltage sag (dashed line), during sag without DSTATCOM (grey line) and during sag with DSTATCOM (black line). For this case, the DSTATCOM takes an average of 2.9 cycles (48 ms) before to inject reactive power.

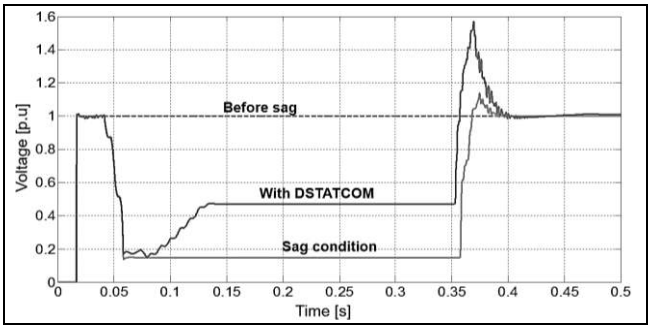

Figure 16. RMS Voltage of phase–A for case 2 (sag at node 842)
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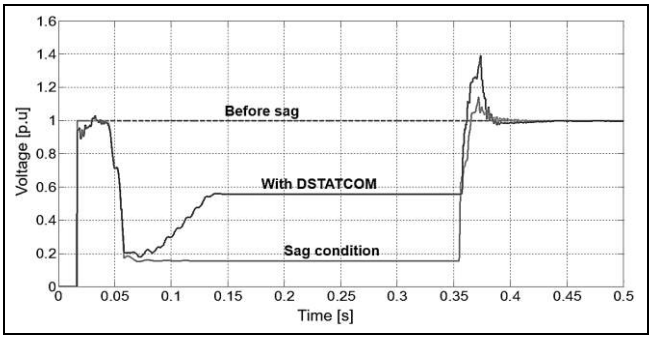

Figure 17. RMS Voltage of phase–B for case 2 (sag at node 842)
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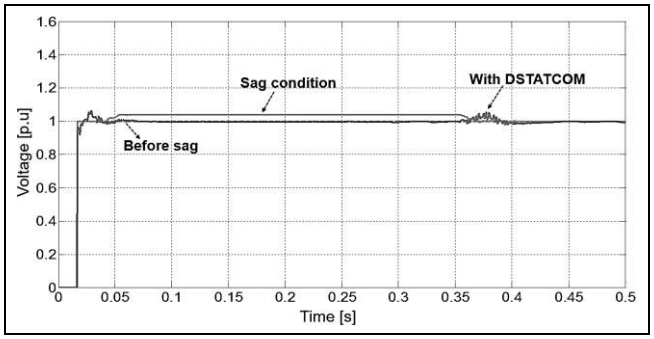

Figure 18. RMS Voltage of phase–C for case 2 (sag at node 842)
Source: Authors

In this case, the DC voltage is varied from 800 V to 3.6 kV and the local function was reduced from 28.49 to 11.71. The RMS voltages per phase at node 842 during the voltage sag condition with and without DSTATCOM are presented in Table 3. Voltages of node 842 are improved with the compensator obtaining an increase of 0.472 p.u. and 0.558 p.u. at phase A and B, respectively. In addition, all voltages of the IEEE-34M system are also improved with values above 0.5 p.u., obtaining a minimum value of 0.512 p.u. at node 830 and a maximum value of 0.778 p.u. at node 802. From these results, the C_{DC} value is 87.3 μF and the injected reactive power of DSTATCOM is 1285 kVAR.

Table 3. Voltage comparison at node 842 for case 2

DSTATCOM Condition	Phase A [p.u]	Phase B [p.u]	Phase C [p.u]
Without DSTATCOM	0.147	0.155	0.998
With DSTATCOM	0.472	0.558	0.999

Source: Authors

Conclusions

In this paper, it was observed that the presence of the DSTATCOM improve the voltage profiles not only in the affected node but also in all voltages of the distribution system. For the cases studies, it was observed that the presence of compensator has a positive effect on the system, contributes to reduce the voltage sags impact and regulates the voltage profiles in all system.

Simulation results show that the DSTATCOM should be installed directly at the bus affected by voltage sag. However, due to the depth of voltage sag conditions analyzed, which were the worst cases in all IEEE-34M test system (average sag of 0.2 p.u.), it is not possible compensate completely the voltage sag.

In addition, a true-48-pulse DSTATCOM model is presented and applied it to the study of power quality problems. The developed features and the graphic advantages available in ATP/EMTP were used to conduct all aspects of the DSTATCOM implementation, the IEEE-34M system modeling and to carry out extensive simulation results.

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