XSICEL 2021

Transición energética en la 4ta revolución industrial

Universidad Tecnológica de Pereira

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DSP-Based Phase Locked Loop Design for Three Phase Grid Synchronization

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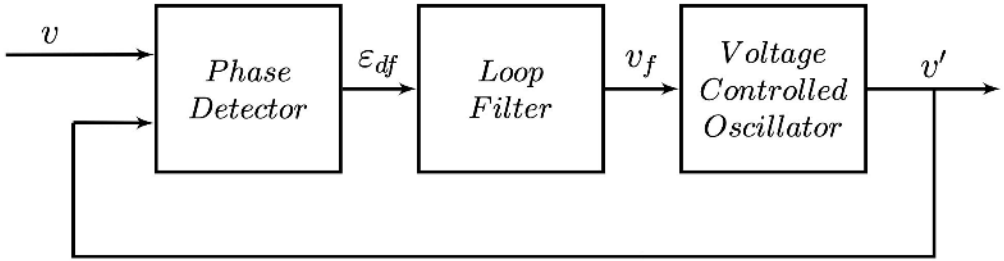
I. Introduction

Is accurate phase angle estimation methods needed for active and reactive power flow (Power Factor) applications?

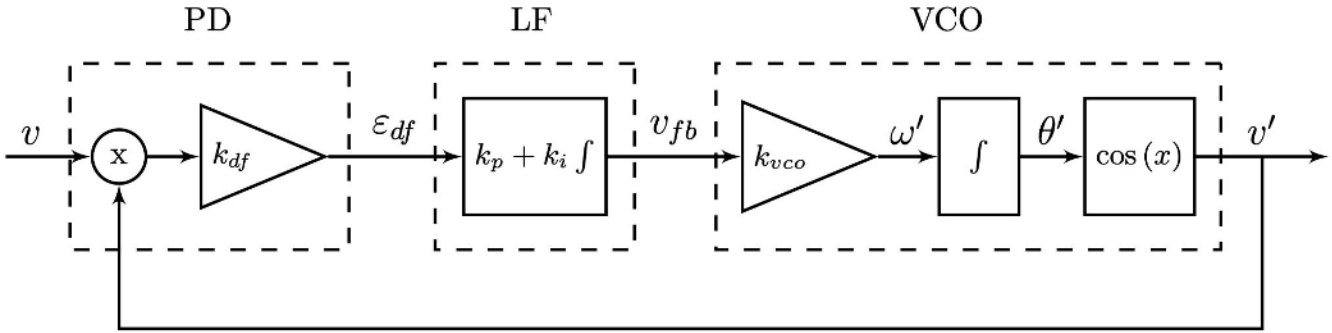
II. Theoretical aspects

Generated a output signal proportional to phase difference (error) and a characteristic of low pass filter for attenuate the components of high frequency and generated the output the same frequency that the reference signal



III. Proposed methodology

Subtitulo



Phase detector

$$E_{df}(s) = \frac{1}{2}\left(\Theta(s) - \Theta'(s)\right)$$

Loop filter

$$V_{fb}(s) = \left(k_p + \frac{k_p}{T_i\, s}\right) E_{df}(s)$$

Voltage Controlled Oscillator

$$\Theta'(s) = \frac{1}{s} V_{fb}(s)$$

III. Proposed methodology

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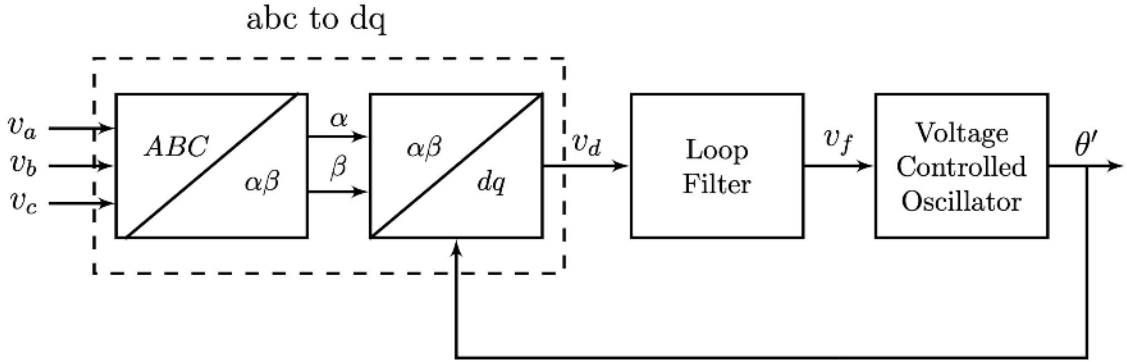
$$LF(z) = \frac{\left(\frac{2k_p + k_i * T}{2}\right) - \left(\frac{2K_p - K_i * T}{2}\right) z^{-1}}{1 - z^{-1}}$$

Based on the discrete function of the low-pass filter block, we proceed to show the DSP implementation of each of the phase tracking loop blocks in pseudocode.

```
void SPLL_1ph_Control(SPLL_1ph *spll)
{
    // Phase Detect
    spll->PD=(spll->AC_input*spll->cos);

    // PI loop filter
    spll->ylf=
          -(spll->lpf.K2*spll->ylf)
          +(spll->lpf.K0_lf*spll->y_pd)
          +(spll->lpf.K1_lf*spll->y_pd);

    // VCO
    spll->wo=spll->wn+spll->ylf;
    spll->theta=spll->theta_old
               +(spll->wo*spll->T);
    spll->cos=cos(spll->theta)


    // Update for next iteration
    spll->ylf_old=spll->ylf;
    spll->theta_old=spll->theta;

}
```

II. Theoretical aspects

Common methods for synchronizing networks proposed in the literature are, open loop model system such as filters, but these model system do not work correctly when the system is unbalanced in voltage source (Voltage).



III. Proposed methodology

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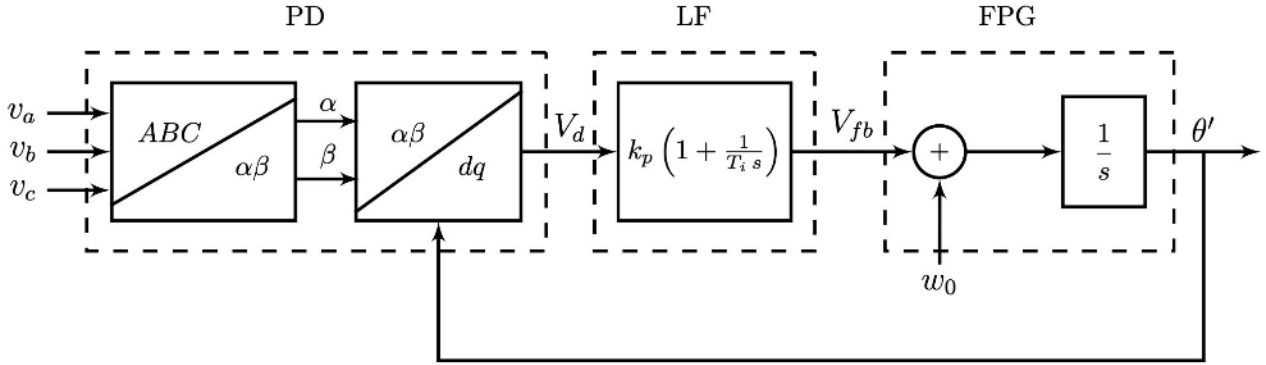

Alpha – Beta transform

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix}$$

Quadrature - Zero transformation

$$\begin{bmatrix} x_d \\ x_q \end{bmatrix} = \begin{bmatrix} cos(\theta) & sin(\theta) \\ -sin(\theta) & cos(\theta) \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix}$$

III. Proposed methodology

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```
void ABC_DQ0(ABC_DQ0 *DQ)
{
    //Reverse Transform - Alpha Beta
    DQ->alpha=(2/3)*(DQ->a-(1/2)
                    *(DQ->b+DQ->c));
    DQ->beta=(2*sqrt(3)/6)*(DQ->b-DQ->c);
    //Park Transform - DQ
    DQ->z=(1/3)*(DQ->a+DQ->b+DQ->c);
    DQ->d=DQ->alpha*DQ->sin
                    -DQ->beta*DQ->cos;
    DQ->q=DQ->alpha*DQ->cos
                    +DQ->beta*DQ->sin;
}
```

The values of the three phases are transformed into the rotating reference frame and the q component is used as phase detection

III. Proposed methodology

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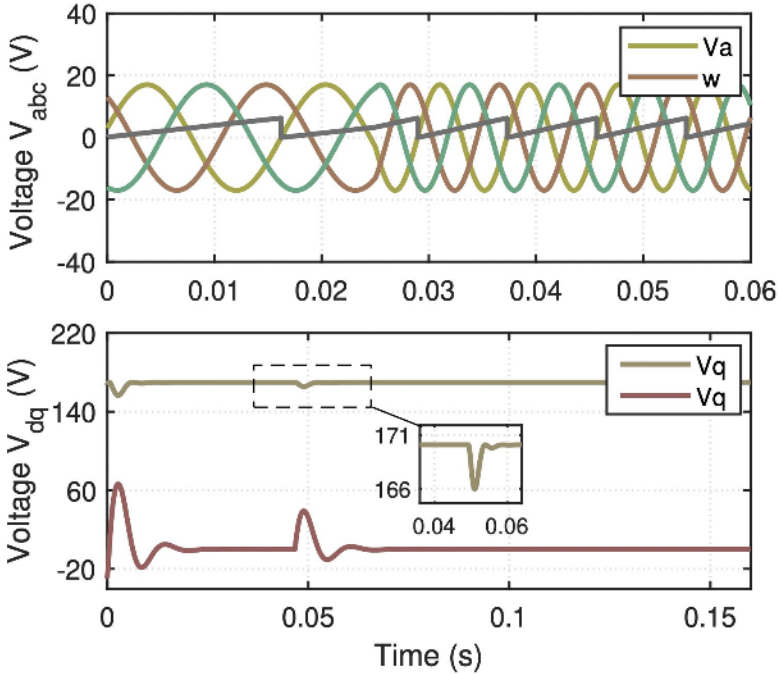
This results in the high-frequency term of the error signal not being taken into account when studying the dynamic response of the phase-locked loop.

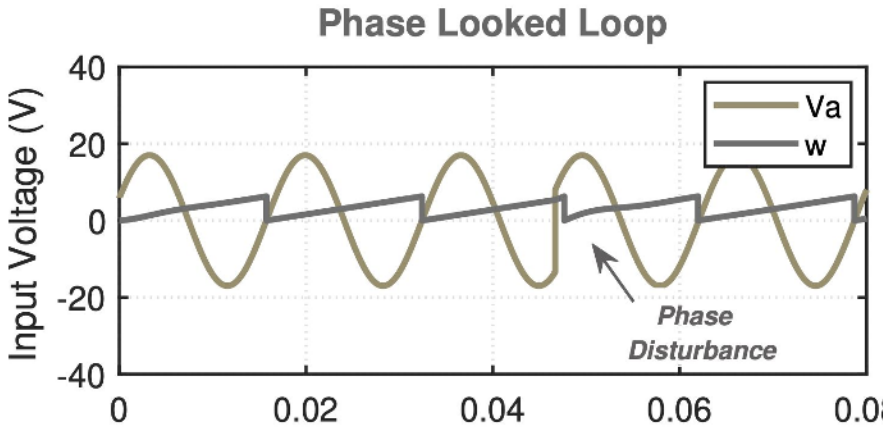
```
void SRFPLL_Control(SFR_PLL *spll)
{
    // Loop Filter
    spll->ylf=spll->ylf_old
            +(spll->lpf.K0*spll->v_q)
            + (spll->lpf.B1*spll->v_q_old);

    // VCO
    spll->fo=spll->fn + spll->ylf;
    spll->theta=spll->theta_old
               +(spll->fo*spll->T)*(2*pi);


    if(spll->theta[0] > 2*pi)
        spll->theta=spll->theta - (2*po);

    // Update for next iteration
    spll->ylf_old=spll->ylf;
    spll->v_q_old=spll->v_q;
    spll->theta_old=spll->theta;
}
```

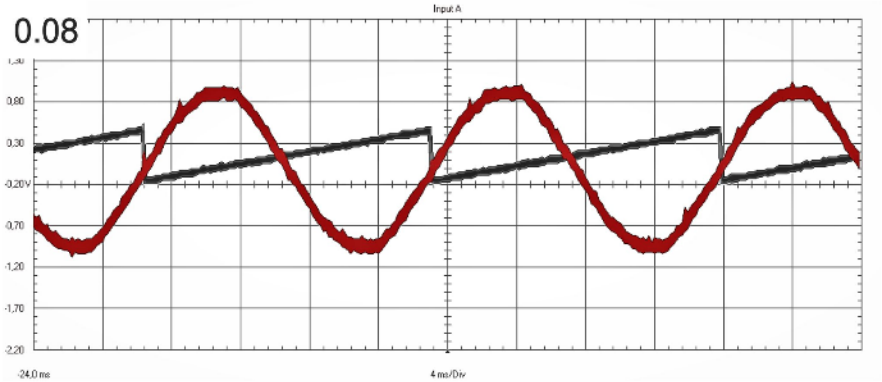
IV. Results



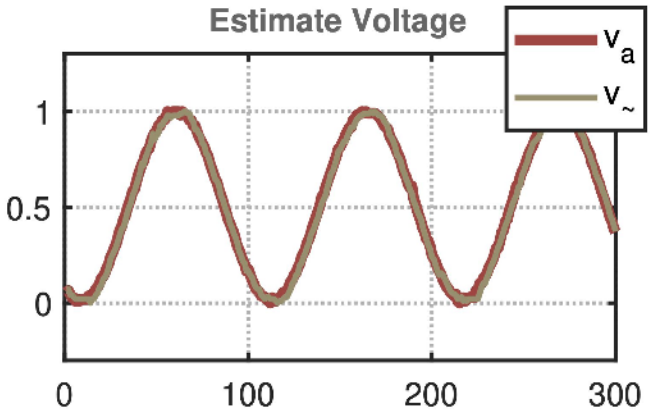
When using Synchronous Reference Framework PLL (SFR PLL), Replaced by the synchronous reference framework PLL they he transform three-phase values `abc' that are variable in time, to constant values in permanent regime

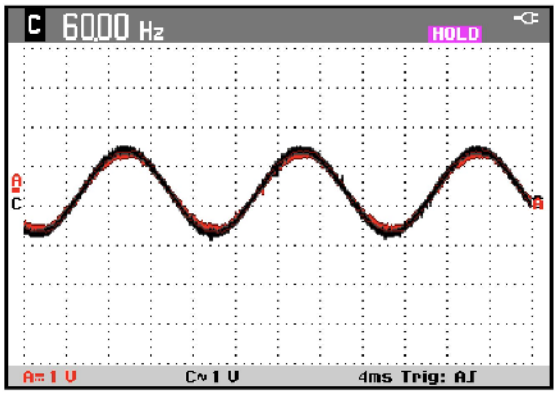
IV. Results


Phase Looked Loop
Input Voltage (V)
40
20
0
-20
-40
0
0.02
0.04
0.06
0.08
Va
w
Phase
Disturbance


Input A
0,80
0,30
-0,20V
-0,70
-1,20
-1,70
-2,20
-24,0 ms
4 ms/Div

IV. Results



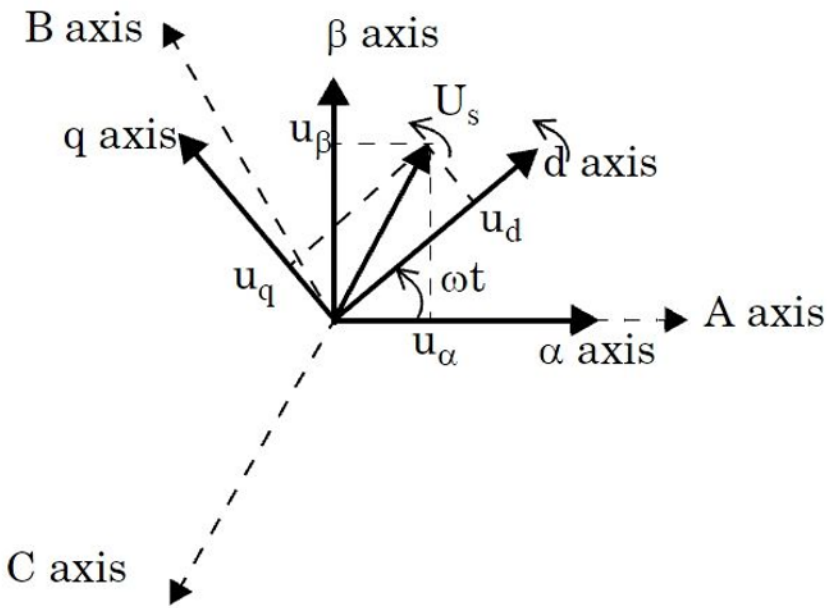


$$RMSE = \sqrt{\frac{1}{n}\sum_{i=1}^{n}(y_i - \hat{y}_i)^2}$$

The data of the estimation and measurement of the line voltage is obtained and a normalization of the same is performed to be compared with the estimation

V. Conclusions

The model system can be implemented in different voltage conditions of input and the simplicity of this structure makes to the system of phase-locked presented be appropriate for the digital implementation.



V. Conclusions

Equally the correct functioning of phase-locked loop with disturbances, demonstrating better yield of estimate of angle respect to other methods propose in the literature and this method follow frequency variations

QUESTIONS ?

VII. References

1. H. S. Kamil, D. M. Said, M. W. Mustafa, M. R. Miveh, and N. Ahmad,"Recent advances in phase-locked loop based synchronization methods for inverter-based renewable energy sources,"Indones. J. Electrical Eng.Comput. Sci, vol. 18, no. 1, pp. 1–8, 2020
2. A. Nicastri and A. Nagliero, "Comparison and evaluation of the plltechniques for the design of the grid-connected inverter systems," in2010 IEEE International Symposium on Industrial Electronics. IEEE,2010, pp. 3865–3870
3. X.-Q. Guo, W.-Y. Wu, and H.-R. Gu, "Phase locked loop and syn-chronization methods for grid-interfaced converters: a review,"PrzegladElektrotechniczny, vol. 87, no. 4, pp. 182–187, 2011
4. F. Shaikh and B. Joseph, "Simulation of synchronous referenceframe pll for grid synchronization using simulink,"IEEE Transactionson Industrial Electronics, pp. 1–6, Dec 2017. [Online]. Available:https://ieeexplore.ieee.org/document/8318790